November 2017

CURRICULUM VITAE
Shahar Kvatinsky

Personal Details:

Born: 1980, Israel
Work Address: Viterbi Faculty of Electrical Engineering
Technion – Israel Institute of Technology
E-Mail: shahar@ee.technion.ac.il
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http://asic2.group

Education:

Ph.D. Electrical Engineering, Technion *2009-2014*
Dissertation Title: "Memristor-based Circuits and Architectures".
Direct track degree.
Advisors: Prof. Avinoam Kolodny, Prof. Eby Friedman, and Prof. Uri Weiser.

MBA Business Administration, the Hebrew University, Jerusalem *2008-2010*
Graduated Magna Cum Laude, GPA: 94.8/100.
Specialized in business strategy and entrepreneurship, and finance and banking.

B.Sc. Computer Engineering and Applied Physics, the Hebrew University, Jerusalem. *2005-2009*
Graduated Magna Cum Laude, GPA: 96.6/100.
Specialized in microelectronics and optoelectronics. My final project was designing and building an integrated system for real-time inline monitoring of pollutants in water, based on E-Coli bacteria under the supervision of Prof. Aharon Agranat. The project won the "Peter Brojde Center for Innovative Engineering and Computer Science" excellence final project 1st prize.
Member of the Dean's honorary list in all four years and won the Dean's reward for excellence twice.

Academic Positions:

Assistant Professor Electrical Engineering, Technion *10/2015-present*
Viterby fellow at the Technion Computer Engineering Center.

Post Doctoral Researcher Computer Science, Stanford University 2014-2015
Working with Professor Mark Horowitz. Development of energy-efficient specialized hardware, primarily for computer vision, computational photography and linear algebra. Also work with Prof. Philip Wong on RRAM design and with Prof. Tsachy Weissman and Dr. Zhiying Wang on coding for RRAM.

Research Interests:

VLSI, computer architecture, digital circuits, analog circuits, memory design, hardware for machine learning, neuromorphic computing, cytomorphic computing, system-on-a-chip, FPGA, hardware-software interface, emerging non-volatile memory technologies, EDA, hardware security.

Professional Experience:

Circuit designer at Intel, Jerusalem. 2007-2009

Designed several IPs, including GPIOs (General Purpose IO), flash comparator, and a bandgap voltage reference. Working especially with SPICE and Verilog.

Honors and Awards:

- Pazy Memorial Research Award for "the most outstanding and original BSF supported project in mathematical and computer sciences" 2017
- Hershel Rich Technion Innovation Award 2017
- Paper selected among top 10 papers in the VLSI-SoC conference to appear in the VLSI-SoC book 2016
- Supervised the Seiden Prize for Multidisciplinary Undergraduate Projects in Nano Electronics 2015
- Viterbi Fellowship in the Center for Computer Engineering at the Technion 2015-2018
- Best Paper of Computer Architecture Letters Award 2015
- Supervised the 3rd place winning project in the Yehoraz Kasher Annual EE Project Contest 2015
- IEEE Guillemin-Cauer Best Paper Award 2015
- Viterbi Fellowship for Nurturing Future Faculty Members 2015
- Hershel Rich Technion Innovation Award 2014
- The Andrew and Erna Finci Viterbi Fellowship 2014
- Vivian Konigsberg Award for Excellence in Teaching (twice) 2013, 2014
- Sanford Kaplan Prize for Creative Management in High Tech in the 21st Century – 1st place 2013
- Best lecturer award – ChipEx 2013 2013
- Supervised the winning project in the Oz Mozes Project Contest 2012
- Intel award for excellence in research 2012
- Vivian Konigsberg Award for Excellence in Teaching (twice) 2011
- Hasso Plattner Institute Fellowship (four years) 2011-2014
- Irwin and Joan Jacobs Fellowship 2011
- Supervised the winning project in the Yehoraz Kasher Annual EE Project Contest 2011
- Sandor Szego Award for Excellence in Teaching (twice) 2010, 2012
- Benin prize for graduate students 2010
- The Marker MBA Case Study Competition finalist 2010
- "Peter Brojde Center for Innovative Engineering and Computer Science" excellence final B.Sc. project prize 2009
- Dean's reward for excellence, Hebrew University (twice) 2007, 2008
- Dean's honorary list, Hebrew University (all four years) 2006-2009

Teaching:

Technion

Lecturer “Seminar in VLSI Systems" (graduate level)	2017-now
Lecturer “Advanced Circuits and Architectures with Memristor" (undergraduate and graduate level)	2016-now
Lecturer (in charge) “Logic Design and Introduction to Computers” (undergraduate level)	2015-now
Lecturer “Advanced Topics in Computer Design: Introduction to Memristors” (graduate level)	2015-2016
Teaching assistant in "Linear Electronics Circuits".	2009-2013
Instructor in SOPC (System on a Programmable Chip) lab.	2009-2014
Supervisor in B.Sc. projects, VLSI laboratory.	2010-2014
Teaching assistant (in charge) in "Computer Architecture".	2011-2014
Teaching assistant (in charge) in "Advanced VLSI Architectures.”	2011-2014

Won six times the Technion excellence award for teaching assistants (Spring 2010, Winter 2011, Spring 2011, Spring 2012, winter 2013, Spring 2014). Supervised the winning projects in the Yehoraz Kasher annual EE project contest in 2011, the Oz Mozes prize in 2012, and the Seiden Prize 2015.

The Hebrew University, Jerusalem.

Instructor in "Physics Lab for Engineers"	2009

Professional Service Activities:

Departmental Activities

Advanced Circuits Research Center (ACRC) – co-director (2016-ongoing).

Editor

Microelectronics Journal (January 2014-ongoing)

Tutorials and Workshops Chair

HPCA 2018.

Program Committee

MDAC in HiPEAC 2017, 2018.
DATE 2018.
MemTCAD in HiPEAC 2015, 2016.
ChipEx 2016.

PhD Committee

1. Robert Gitterman, Bar Ilan University, 2016.
2. Evripides Kyriakides, University of Nicosia, Cyprus, 2016.
3. Roman Kaplan, Technion, 2017.
4. Oron Port, Technion, 2017.

MSc Committee

1. Amit Kazimirsky, Bar Ilan University, 2016.
2. Kfir Mizrahi, Technion, 2017.

3. Oren Nishri, Technion, 2017.

Workshop, Tutorials, and Training School Organizer

- "In-Memory and In-Storage Computing with Emerging Technologies," in PACT 2016 (with Leonid Yavits, Technion).
- "2017 Stephen and Sharon Seiden Frontiers in Engineering and Science Workshop: Beyond CMOS: From Devices to Systems," June 2017, Technion (with Eby Friedman, University of Rochester and Avinoam Kolodny, Technion).
- EU COST Action IC-1401 training school, June 2017, Haifa, Israel.
- "Mixed Signal Circuit Design with Memristors," tutorial in IEEE COMCAS, November 2017.

Special Session Organizer

- "Memristors for Computing," in CNNA 2016 (with Dietmar Fey, FAU).
- "Computing with Memristors" in DATE 2017 (with Said Hamdioui, TU Delft, and Gert Cauwenberghs, UCSD)

Scientific Advisory Board

- Chua Memristor Center (CMC) at TU Dresden, Germany.
- International Advisory Board of the 3rd International Conference "Emerging Materials, Technologies and Applications for Non-volatile Memory Devices"

Journal/Conference Referee

1. 17th International Conference on Digital Signal Processing (DSP 2011).
2. 39th International Symposium on Computer Architecture (ISCA 2012).
3. Microelectronics Journal.
4. IEEE Transactions on Nanotechnology.
5. 7th International Symposium on Networks-on-Chip (NOCS 2013).
6. Reed-Muller Workshop (RM 2013).
7. IEEE International Symposium on Circuits and Systems (ISCAS) 2013.
8. Radioengineering.
9. PLOS ONE.
10. IEEE International Symposium on Circuits and Systems (ISCAS) 2014.
11. IEEE Transactions on Electron Devices.
12. Journal of Circuits, Systems, and Computers.
13. IEEE Transactions on Circuits and Systems I: Regular Papers.
14. IEEE Transactions on Circuits and Systems II: Express Briefs.
15. IEEE Transactions on Very Large Scale Integration (VLSI).
16. IEEE Transactions on Neural Networks and Learning Systems.
17. IEEE Journal on Emerging and Selected Topics in Circuits and Systems.
18. International Journal of Electronics and Communications.
19. IEEE Electron Device Letters.
20. Frontiers in Neuroscience.
21. The 48th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO 2015).
22. BIOCAS 2015.
23. IEEE International Symposium on Circuits and Systems (ISCAS) 2016.
24. IEEE Transactions on Computer-Aided Design.
25. IEEE Transactions on Emerging Topics in Computing.
26. ACM Journal on Emerging Technologies in Computing Systems.

27. IET Circuits, Devices, & Systems.
28. International Workshop on Cellular Nanoscale Networks and their Applications (CNNA) 2016.
29. Neural Computing and Applications (NCAA).
30. IEEE International Symposium on Circuits and Systems (ISCAS) 2017.
31. Electronics Letters.
32. High Performance Computer Architecture (HPCA) 2018.

Membership in Professional Societies:

IEEE (member).

Military Service:

Officer in the IDF, rank: Lieutenant Colonel. 1999-2004

Participated in several courses and training including sergeant course, officer course, and company commander course and served in several commanding positions including an artillery battery commander and artillery officer course commander.

Currently in the reserve forces.

Students Supervised

Completed MSc theses

1. Yifat Levy, "Logic with Memristive Akers Arrays" (co-advisors A. Kolodny and E. Friedman, Graduated 2015, currently with Intel).
2. Misbah Ramadan, "Adaptive Programming for Multi-Level Cell ReRAM," (co-advisor R. Ginosar, graduated 2017, currently with Apple).

Current Post-docs

1. John Reuben, 2017-now.

PhD theses in progress

1. Loai Daniel, “Neuromorphic Computing with Memristors” (started 2015, expected graduation 2019).
2. Rotem Ben-Hur, “Logic within the Memory” (started 2015, expected graduation 2020).
3. Nicolas Wainstein, "RF Front-End Circuits Based on Memristive Devices" (started 2016, expected graduation 2020).
4. Ben Perach (started 2017, expected graduation 2021).

MSc theses in progress

5. Ameer Haj Ali (started 2016, expected graduation 2018).
6. Tzofnat Greenberg, "Memristive Artificial Neural Network Accelerator with Online Training (started 2016, expected graduation 2018).
7. Nishil Talati, "Logic Design for non-von Neumann Architectures using Memristors" (started 2016, expected graduation 2018).

8. Nimrod Wald, “Memristor Aided Logic within the Memory” (started 2015, expected graduation 2018).

B.Sc. Projects

1. Dmitry Belousov and Slavik Liman, "Memristor-based Circuits" (*Winners of the Yehoraz Kasher EE Project Contest*).
2. Zahi Lahti and Elad Osherov, "Memristor Model."
3. Oren Lev and Emanuel Darji, "Analysis of Power Grids."
4. Keren Talisveyberg and Dmitry Fliter, "Memristor Verilog-A and MATLAB Modeling."
5. Ilan Shusterman and Michael Rozenblat, "Memristor-based Memory Analysis."
6. Leon Karbachevsky and Boaz Blankrot, "Memristor-based Analog Circuits."
7. Guy Satat and Nimrod Wald, "Memristor-based Full Adder," "Memristor-based Multithreading Processor" (*Winners of the Oz Mozes Project Contest*).
8. Boris Bashkansky and Lahav Madlinsky, "Memristor-based Memory Array Circuit and Layout Design."
9. Rotem Tabach and Dina Leshinsky, "Neuromorphic Systems."
10. Yiffah Fishler and Shir Lindenbaum, "Memristor Modeling."
11. Firas Shama and Louie Matar, "Memristor-based Multithreading Processor."
12. Keren Tendeter and Shiran Shuster, "Simulator for Memristor-based Memory."
13. Misbah Ramadan and Loai Danial, "Analysis of a Memristor-based Crossbar."
14. Hani Bezalel and Rotem Gabay, "Controller for Memristor-based Logic."
15. Benny Fellman and Gilad Tsoran, "Memristor-based Multithreading Processor."
16. Moab Arar and Muhammad Grefat, "Simulation Tools for Emerging Memory Technologies."
17. Israel Goldstein and Alex Dozortzev, "Memristor-based Crossbar for Neural Networks."
18. Misbah Ramadan, "Memristor Modeling."
19. Yoav Furman and Rula Naffaa, "Complementary MRL."
20. Avishay Drori and Elad Amrani, "Logic Design with Memristive Devices."
21. Eyal Rosenthal and Sergey Greshnikov, "Machine Learning with Memristors."
22. Itay Tsabari, "DNA Sequencing by Logic within Memory."

Research Grants:

1. HiPER Consortium – Israel Ministry of Economics (2016-2018, 470K NIS for two years).
2. KAMIN project no. 57681 – "Analog to Digital Converters with Memristive Neural Network" (2016-2017, 439,480 NIS for one year).
3. Intel Collaborative Research Institute – Computational Intelligence: Memory Intensive Architectures (2015-2017, $137.5K for two years).
4. ICT COST action IC1401 – "Memristors – Devices, Models, Circuits, Systems and Applications (MemoCIS)" (2015-2018).
5. NSF-BSF proposal no. 2015709, "Dynamically Configurable Memory Technology Based on Ferroelectric-Gated FET’s (FeFET’s) (2017-2019, Co-PI with Moshe Eizenberg, Technion and Ma Tso-Ping, Yale University, $150K for three years).
6. Russell Berrie Nanotechnology Institute Nevet grant, "Integrated Genetics and Nanoelectronics Breaking through the Scaling Limits of Moore's Law," (2017-2018, co-PI with Ramez Danial, Technion, $40K for two years).

7. Cisco University Research Program Fund, "Vulnerability Analysis of Emerging Nonvolatile Memory Technologies," lead PI (2017, co-PI Prof. Avi Mendelson, Technion, $80K for one year).
8. United States – Israel Binational Science Foundation (BSF) grant, "High-Performance Normally-Off Parallel Processing," (2017-2019, co-PI with Pierre-Emmanuel Gaillardon, University of Utah, $150K for two years).
9. European Research Council Starting Grant, "Memristive In-Memory Processing Systems" (2017-2023, 1.5 Million Euro for 5 years).
10. Israel Science Foundation grant no. 1514/17, "Design of Computer Memories with Independent Computing Capabilities," (2017-2021, 1,023,612 ILS for 4 years).
11. Israel Science Foundation equipment grant for new faculty no. 1515/17 (758,517 ILS).
12. Ministry of Science and Technology, "Integrated Genetics and Memristors breaking through the scaling limits of Moore's law" (2017-2020, 1,555,329 ILS for 3 years, Co-PI with Ramez Daniel, Technion).

PUBLICATIONS

Thesis

S. Kvatinsky, "Memristor-Based Circuits and Architectures," PhD dissertation, August 2014.

Book Chapters:

1. N. Wald, E. Amrany, A. Drory, and **S. Kvatinsky**, "Logic with Unipolar Memristors: Circuits and Design Methodology," *VLSI-SoC: System-on-Chip in the Nanoscale Era – Design, Verification and Reliability*, IFIP Advances in Information and Communication Technology, T. Hollstein, J. Raik, S. Kostin, A. Tšertov, I. O'Connor, R. Reis (Eds.), Springer, Vol. 508, Chapter 2, pp. 24-40, 2017.
2. J. Reuben, R. Ben Hur, N. Wald, N. Talati, A. Haj Ali, P.-E. Gaillardon, and **S. Kvatinsky**, "A Taxonomy and Evaluation Framework for Memristive Logic," *Handbook of Memristor Networks*, Springer (submitted).
3. N. Talati, R. Ben-Hur, N. Wald, A. Haj Ali, J. Reuben, and **S. Kvatinsky**, "mMPU – A Real Processing-in-Memory Architecture to Combat the von Neumann Bottleneck," *Advanced Applications of Emerging NVM devices*, The Springer Series in Advanced Microelectronics, Springer (submitted).

Refereed Journal Papers:

4. N. Wainstein and **S. Kvatinsky**, "A Lumped RF Model for Nanoscale Memristive Devices and Non-Volatile Single-Pole Double-Throw Switches," *IEEE Transactions on Nanotechnology*, (in press).
5. L. Danial, N. Wainstein, S. Kraus, and **S. Kvatinsky**, "DIDACTIC: A Deeply Intelligent Digital-to-Analog Converter with a Trainable Integrated Circuit using Memristors," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems* (in press).
6. N. Wainstein and **S. Kvatinsky**, "TIME – Tunable Inductors using MEmristors," *IEEE Transactions on Circuits and Systems I: Regular Papers*, (in press).
7. A. Doz, I. Goldstein, and **S. Kvatinsky**, "Analysis of the Row Grounding Method in a Memristor-Based Crossbar Array," *International Journal of Circuit Theory and Applications* (in press).

8. Y. Cassuto, **S. Kvatinsky**, and E. Yaakobi, "Information-Theoretic Sneak Path Mitigation in Memristor Crossbar Arrays," *IEEE Transaction on Information Theory*, Vol. 62, No. 9, pp. 4801-4814, September 2016.
9. N. Talati, S. Gupta, P. Mane, and **S. Kvatinsky**, "Logic Design within Memristive Memories Using Memristor Aided loGIC (MAGIC)," *IEEE Transactions on Nanotechnology*, Vol. 15, No. 4, pp. 635-650, July 2016.
10. A. Morad, L. Yavits, **S. Kvatinsky**, and R. Ginosar, "Resistive GP-SIMD Processing In-Memory," *ACM Transactions on Architecture and Code Optimization*, Vol. 12, No. 4, Article 57, January 2016.
11. L. Yavits, **S. Kvatinsky**, A. Morad, and R. Ginosar, "Resistive Associative Processor," *IEEE Computer Architecture Letters*, Vol. 14, No. 2, July-December 2015. ***Best of CAL winner 2015***.
12. D. Soudry, D. Di Castro, A. Gal, A. Kolodny, and **S. Kvatinsky**, "Memristor-based Multilayer Neural Networks with Online Gradient Descent Training," *IEEE Transactions on Neural Networks and Learning Systems*, Vol. 26, No. 10, pp. 2408-2421, October 2015.
13. R. Patel, **S. Kvatinsky**, E. G. Friedman, and A. Kolodny, "Multistate Register Based on Resistive RAM," *IEEE Transactions on Very Large Scale Integration (VLSI)*, Vol. 23, No. 9, pp. 1750-1759, September 2015.
14. **S. Kvatinsky**, M. Ramadan, E. G. Friedman, and A. Kolodny, "VTEAM – A General Model for Voltage Controlled Memristor," *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 62, No. 8, pp. 786-790, August 2015.
15. Y. Levy, J. Bruck, Y. Cassuto, E. G. Friedman, A. Kolodny, E. Yaacobi, and **S. Kvatinsky**, "Logic Operation in Memory Using a Memristive Akers Array," *Microelectronics Journal*, Vol. 45, No. 11, pp. 1429-1437, November 2014.
16. **S. Kvatinsky**, D. Belousov, S. Liman, G. Satat, N. Wald, E. G. Friedman, A. Kolodny, and U. C. Weiser, "MAGIC – Memristor Aided LoGIC," *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 61, No. 11, pp. 895-899, November 2014.
17. **S. Kvatinsky**, N. Wald, G. Satat, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Memristor-Based Material Implication (IMPLY) Logic: Design Principles and Methodologies," *IEEE Transactions on Very Large Scale Integration (VLSI)*, Vol. 22, No. 10, pp. 2054-2066, October 2014.
18. **S. Kvatinsky**, Y. H. Nacson, Y. Etsion, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Memristor-Based Multithreading," *IEEE Computer Architecture Letters*, Vol. 13, No. 1, pp. 41-44, January-June 2014.
19. **S. Kvatinsky**, E. G. Friedman, A. Kolodny, and U. C. Weiser, "TEAM - ThrEshold Adaptive Memristor Model," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 60, No. 1, pp. 211-221, January 2013. ***2015 IEEE Guillemin-Cauer Best Paper Award.***

Submitted Refereed Journal Papers:

20. T. Greenberg, A. Haj Ali, and **S. Kvatinsky**, "Supporting the Momentum Algorithm Using a Memristor-Based Synapse,", (submitted).
21. M. Ramadan, R. Ginosar, and **S. Kvatinsky**, "Adaptive Programming in Multi-Level Cell ReRAM," (submitted).

Refereed Conference Papers:

22. R. Ben Hur, N. Wald, N. Talati, and **S. Kvatinsky**, "Synthesis and Mapping of Boolean Functions for Memristor Aided Logic (MAGIC)," *Proceeding of the IEEE International Conference on Circuits Aided Design*, November 2017 (in press).
23. H. Abu Hanna, L. Danial, **S. Kvatinsky,** and R. Daniel, "Modeling Biochemical Reactions and Gene Networks with Memristors," *Proceeding of the IEEE Symposium on Biological Circuits and Systems*, October 2017 (in press).
24. J. Reuben, R. Ben Hur, N. Wald, N. Talati, and **S. Kvatinsky**, "Memristive Logic: A Framework for Evaluation and Comparison," *Proceeding of the IEEE International Symposium on Power and Timing Modeling, Optimization and Simulation*, September 2017 (in press).
25. N. Wainsten and **S. Kvatinsky**, "An RF Memristor Model and Memristive Single-Pole Double Throw Switches," *Proceeding of the IEEE International Symposium on Circuits and Systems*, May 2017 (in press).
26. N. Talati, Z. Wang, and **S. Kvatinsky,** "Rate-Compatible and High-Throughput Architecture Designs for Encoding LDPC Codes," *Proceeding of the IEEE International Symposium on Circuits and Systems*, May 2017 (in press).
27. L. Azriel and **S. Kvatinsky**, "Towards a Memristive Hardware Secure Hash Function (MemHash)", *Proceedings of the IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, May 2017 (in press).
28. **S. Kvatinsky**, R. Ben-Hur, N. Talati, and N. Wald, "mMPU: Memristive Memory Processing Unit," *International Conference on Memristive Materials, Devices & Systems*, April 2017.
29. S. Hamdioui, **S. Kvatinsky**, G. Cauwenberghs, L. Xie, K. Bertels, N. Wald, S. Joshi, H. M. Elsayed, and H. Corporaal, "Memristor For Computing: Myth or Reality?" *Proceedings of the Design, Automation and Testing in Europe*, pp. 722-731, March 2017.
30. N. Wald and **S. Kvatinsky**, "Design Methodology for Stateful Memristive Logic Gates", *Proceedings of the IEEE International Conference on Science of Electrical Engineering*, November 2016 (in press).
31. R. Ben-Hur and **S. Kvatinsky**, "Memristive Memory Processing Unit (MPU) Controller for In-Memory Processing", *Proceedings of the IEEE International Conference on Science of Electrical Engineering*, November 2016 (in press).
32. H. Ha, A. Pedram, S. Richardson, **S. Kvatinsky**, and M. Horowitz, "Improving Energy Efficiency of DRAM by Exploiting Half Page Row Access," *Proceedings of the Annual ACM/IEEE International Symposium on Microarchitecture*, pp. 1-12, October 2016.
33. A. Vasilyev, N. Bhagdikar, S. Richardson, A. Pedram, **S. Kvatinsky**, and M. Horowitz, "Evaluating Programmable Architectures for Image and Vision Applications," *Proceedings of the Annual ACM/IEEE International Symposium on Microarchitecture*, pp. 1-13, October 2016.
34. E. Amrany, A. Drory, and **S. Kvatinsky**, "Logic Design with Unipolar Memristors," *Proceedings of the IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, September 2016 (in press). ***Selected for post-conference book (top 10 papers).***
35. R. Ben-Hur, N. Talati, and **S. Kvatinsky**, "Algorithmic Considerations in Memristive Memory Processing Units (MPU)," *Proceedings of the International Cellular Nanoscale Networks and their Applications*, August 2016 (in press).

36. R. Ben-Hur and **S. Kvatinsky**, "Memory Processing Unit for In-Memory Processing," *Proceedings of the IEEE/ACM International Symposium on Nanoscale Architectures*, pp. 171-172, July 2016.
37. Y. Cassuto, **S. Kvatinsky**, and E. Yaakobi, "Write Sneak-Path Constraints Avoiding Disturbs in Memristor Crossbar Arrays," *Proceedings of the IEEE International Symposium on Information Theory*, pp. 950-954, July 2016.
38. E. Rosenthal, S. Greshnikov, D. Soudry, and **S. Kvatinsky**, "A Fully Analog Memristor-Based Multilayer Neural Network with Online Backpropagation Training," *Proceeding of the IEEE International Symposium on Circuits and Systems*, pp. 1394-1397, May 2016.
39. M. Ramadan, **S. Kvatinsky**, and R. Ginosar, "Memristor Modeling," *Proceedings of the Workshop on Memristor Technology, Design, Automation and Computing*, January 2016.
40. L. Danial and **S. Kvatinsky**, "Memristive Artificial Neural Networks Based Analog to Digital Converter (ADC)," *Proceedings of the Workshop on Memristor Technology, Design, Automation and Computing*, January 2016.
41. R. Ben-Hur and **S. Kvatinsky**, "Processing within a Memristive Memory," *Proceedings of the Workshop on Memristor Technology, Design, Automation and Computing*, January 2016.
42. Z. Jiang, P. Huang, L. Zhao, **S. Kvatinsky**, S. Yu, X. Liu, J. Kang, Y. Nishi, and H.-S. P. Wong, "Analysis and Predication on Resistive Random Access Memory (RRAM) 1S1R Array," *Proceedings of the 2015 International Memory Workshop*, pp. 1-4, May 2015.
43. **S. Kvatinsky**, Y. H. Nacson, R. Patel, Y. Etsion, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Memristive Multistate Pipeline Register," *Proceedings of the International Cellular Nanoscale Networks and their Applications*, pp. 1-2, July 2014.
44. Y. Cassuto, **S. Kvatinsky**, and E. Yaakobi, "On the Channel Induced by Sneak-Path Errors in Memristor Arrays," *Proceedings of the International Conference on Signal Processing and Communication*, pp. 1-6, July 2014.
45. **S. Kvatinsky**, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Memory Intensive Computing," *Proceeding of the Annual Non-Volatile Memories Workshop*, March 2014.
46. Y. Cassuto, **S. Kvatinsky**, and E. Yaakobi, "Sneak-Path Constraints in Memristor Crossbar Arrays," *Proceedings of the IEEE International Symposium on Information Theory*, pp. 156-160, July 2013.
47. Y. Cassuto, **S. Kvatinsky**, and E. Yaakobi, "Sneak-Path Constraints in Memristor Crossbar Arrays," *Proceeding of the Annual Non-Volatile Memories Workshop*, March 2013.
48. **S. Kvatinsky**, K. Talisveyberg, D. Fliter, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Models of Memristors for SPICE Simulations," *Proceedings of the IEEE Convention of Electrical and Electronics Engineers in Israel*, pp. 1-5, November 2012.
49. **S. Kvatinsky**, N. Wald, G. Satat, E. G. Friedman, A. Kolodny, and U. C. Weiser, "MRL – Memristor Ratioed Logic," *Proceedings of the International Cellular Nanoscale Networks and their Applications*, pp. 1-6, August 2012.
50. **S. Kvatinsky**, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Memristor-based IMPLY Logic Design Flow," *Proceedings of the IEEE International Conference on Computer Design*, pp.142-147, October 2011.

51. **S. Kvatinsky**, E. G. Friedman, A. Kolodny, and L. Schächter, "Power Grid Analysis Based on a Macro Circuits Model", *Proceedings of the IEEE Convention of Electrical and Electronics Engineers in Israel,* pp. 708-712, November 2010.

Submitted Refereed Conference Papers:

52. A. Haj Ali, R. Ben-Hur, N. Wald, and **S. Kvatinsky**, "Efficient Algorithms for In-memory Fixed Point Multiplication Using MAGIC," (submitted).

Magazines:

53. R. Daniel and **S. Kvatinsky**, "Combining Biology and Electronics Using Emerging Memristive Technologies," *Tower Jazz Technical Journal*, Vol. 8, pp. 30-38, June 2017.
54. A. Pedram, S. Richardson, S. Galal, **S. Kvatinsky**, and M. Horowitz, "Dark Memory and Accelerator-Rich System Optimization in the Dark Silicon Era", *IEEE Design and Test*, Vol. 34, No. 2, pp. 39-50, April 2017.
55. **S. Kvatinsky**, E. G. Friedman, A. Kolodny, and U. C. Weiser, "The Desired Memristor for Circuit Designers," *IEEE Circuits and Systems Magazine*, Vol. 13, No. 2, pp. 17-22, second quarter 2013.

Technical Reports:

56. R. Ben Hur, N. Wald, N. Talati, and **S. Kvatinsky**, " Latency Optimized Mapping of Logic Functions for Memristor Aided Logic (MAGIC)," *CCIT Technical Report #908*, December 2016.
57. X. Yang, J. Pu, B. B. Rister, N. Bhagdikar, J. Ragan-Kelley, S. Richardson, **S. Kvatinsky**, A. Pedram, and M. Horowitz, "A Systematic Approach to Blocking Convolutional Neural Networks," *ArXiv:1606.04209*, June 2016.
58. **S. Kvatinsky**, M. Ramadan, E. G. Friedman, and A. Kolodny, "VTEAM - A General Model for Voltage Controlled Memristors," *CCIT Technical Report #*856, April 2014.
59. D. Soudry, D. Di Castro, A. Gal, A. Kolodny, and **S. Kvatinsky**, "Hebbian Learning Rules with Memristors," *CCIT Technical Report #*840, September 2013.
60. **S. Kvatinsky**, E. G. Friedman, A. Kolodny, and U. C. Weiser, "TEAM - ThrEshold Adaptive Memristor Model," *CCIT Technical Report #80*4, January 2012.
61. **S. Kvatinsky**, K. Talisveyberg, D. Fliter, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Verilog-A for Memristor Models," *CCIT Technical Report #801*, December 2011.
62. **S. Kvatinsky**, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Memristor-based IMPLY Logic Design Flow," *CCIT Technical Report #795*, August 2011.

Patents:

1. S. Kvatinsky, Y. Levy, and A. Kolodny, "Memristive Akers Logic Array," US patent no. 9548741.
2. A. Kolodny, S. Kvatinsky, R. Patel, and E. G. Friedman, "Multistate Register Having a Flip Flop and Multiple Memristive Devices," US patent no. 9679650 B2.
3. S. Kvatinsky, D. Belousov, S. Liman, and G. Satat, "A Pure Memristive Logic Array," US patent no. 9685954.
4. D. Soudry, S. Kvatinsky, A. Gal, D. Di Castro, and A. Kolodny, "Implementating multiplication in adaptive circuits using memristive devices," US patent no. 9754203.

5. S. Kvatinsky, A. Kolodny, and U. C. Weiser, "Memristor-Based Multithreading," Israel patent application no. 225988.
6. S. Kvatinsky, A. Kolodny, and U. C. Weiser, "Memristor-Based Multithreading," US patent application no. 14/219,030.
7. A. Morad, L. Yavits, S. Kvatinsky, and R. Ginosar, "A Hybrid Processor," US patent application no. 14/979,880.
8. A. Drori, E. Amrani, and S. Kvatinsky, "Implementation of Logic Circuits with Unipolar Memristive Devices, Thin Film Resistive Switches, and Phase Change Memory," US patent application no. 62/340,559.
9. M. Ramadan, S. Kvatinsky, and R. Ginosar, "Adaptive Programming for Memories with Multi-Level Cells," US patent application no. 62/432,615.
10. L. Azriel and S. Kvatinsky, "MemHash: a Memristive Hardware Secure Hash Function," US patent application no. 62/492,246.

Selected Talks (including plenary, keynote, and invited):

SIMPLE MAGIC:

- EPFL Workshop on Logic Synthesis and Emerging Technologies, Lausanne, Switzerland, September 2017 (invited).

Memory Intensive Architectures

- Intel, Hillsborough, OR, USA, June 2017 (invited).

mMPU: Memristor Memory Processing Unit

- 2017 Stephen and Sharon Seiden Frontiers in Engineering and Science Workshop: Beyond CMOS: From Devices to Systems, Technion, Haifa, Israel, June 2017.
- Intel Collaborative Research Institute - Computational Intelligence Retreat, Haifa, Israel May 2017 (invited).

Memristors for Learning

- IEEE International Conference on Science of Electrical Engineering, November 2016 (invited).

Computation with Memristors

- Intel, Haifa, Israel, December 2016.
- MemoCIS workshop, Palma de Mallorca, Spain, September 2016 (invited).

Introduction to Memristors

- ChipEx 2016, Tel Aviv, May 2016 (invited).

Avoiding the Dark Ages with Memristors

- MemoCIS Workshop: "Memristors: at the Crossroad of Devices and Applications", Milan, March 2016 (keynote).

Emerging Memory Technologies: Challenges and Opportunities

- DesignEx 2015, Tel Aviv, November 2015 (invited).

Designing Extremely Energy Efficient Computers with Memristors

- 3rd Green Photonics Symposium, Technion, Haifa, Israel, March 2016.
- UT Dresden, Dresden, Germany, February 2016 (invited).
- Qualcomm, Haifa, Israel, January 2016.
- Mellanox, Yokneham, Israel, December 2015.
- Marvell, Petach Tikva, Israel, November 2015.
- Qualcomm, San Diego, July 2015.
- ARM, San Jose, CA, June 2015.
- UCLA, Los Angeles, CA, June 2015 (invited).
- UC Santa Barbara, Santa Barbara, CA, June 2015 (invited).

- Nvidia Research, Santa Clara, CA, May 2015.
- Intel Labs, Hillsborough, OR, May 2015.

Designing Extremely Energy Efficient Computers

- UT Austin, Austin, TX, March 2015 (invited).
- Technion – Israel Institute of Technology, Haifa, Israel, January 2015.
- Hebrew University of Jerusalem, Jerusalem, Israel, January 2015.
- Ben Gurion University of the Negev, Beer Sheva, Israel, January 2015.

Memory Intensive Computing

- Tel Aviv University, Tel Aviv, July 2014.
- *DATE 2014*, Dresden, Germany, March 2014.
- *HiPEAC 2014*, Vienna, Austria, January 2014.

Building the Computers of the Future – a Talk about Resistors, Memories, and More

- *Jacobs Showcase Lecture Series: Much is New Under the Sun,* Technion - Israel Institute of Technology, Haifa, Israel, November 2013.

Memristors – Not Only Memory

- Princeton University, NJ, September 2013.
- Columbia University, NY, September 2013.
- Stanford University, Stanford, CA, September 2013.
- UC Berkeley, Berkeley, CA, September 2013.
- HP Labs, Palo Alto, CA, September 2013.
- UC San Diego, La Jolle, CA, September 2013.
- UC Santa Barbara, Santa Barbara, CA, October 2013.
- *The International Conference of the Israeli Semiconductor Industry (ChipEx 2013)*, Tel Aviv, Israel, May 2013. **Best lecture award**.

The Desired Memristor for Circuit Designers

- *Nature Conference on "Frontiers in Electronic Materials: Correlation Effects and Memristive Phenomena*," Aachen, Germany, June 2012.

Memristor-based Logic Circuit Design

- *IEEE/ACRC Workshop on Memristors and Resistive Memory Devices and Applications in Computer Architecture and Brain-Inspired Systems*, Technion - Israel Institute of Technology, Haifa, Israel, March 2012.

Memristors and Related Applications

- *The International Conference of the Israeli Semiconductor Industry (ChipEx 2011)*, Tel Aviv, Israel, May 2011.

Posters:

1. N. Wainstein and **S. Kvatinsky**, "RF Memristor Modeling," *International Conference on Memristive Materials, Devices & Systems*, April 2017.
2. R. Ben-Hur and **S. Kvatinsky**, "Processing within a Memristive Memory," *Proceedings of the International Workshop on Emerging Memory Solutions*, *DATE Conference*, March 2016.
3. D. Soudry, D. Di Castro, A. Gal, A. Kolodny, and **S. Kvatinsky**, "Implementing Hebbian Learning Rules with Memristors," *Workshop on "Memristor-based Systems for Neuromorphic Applications,"* September 2013.
4. **S. Kvatinsky**, E. G. Friedman, A. Kolodny and U.C. Weiser, "Memristor-based Logic," *MemCo Workshop - Memristors for Computing*, November 2012.

5. **S. Kvatinsky**, E. G. Friedman, A. Kolodny and U.C. Weiser, "Memristor-based Circuits and Architectures," *2nd Technion Computer Engineering (TCE) Conference*, June 2012.
6. **S. Kvatinsky**, E. G. Friedman, A. Kolodny and U.C. Weiser, "Memristor-based Applications," *1st Technion Computer Engineering (TCE) Conference*, June 2011.