28th July 2019

CURRICULUM VITAE
Shahar Kvatinsky

Personal Details

Work Address: Viterbi Faculty of Electrical Engineering
Technion – Israel Institute of Technology
Haifa 3200003
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http://asic2.group

Academic Degrees

2014 *Ph.D. Electrical Engineering, Technion*
Dissertation Title: "Memristor-based Circuits and Architectures".
Direct track degree.
Advisors: Prof. Avinoam Kolodny, Prof. Eby Friedman, and Prof. Uri Weiser.

2010 *MBA Business Administration, Hebrew University, Jerusalem*
Graduated Magna Cum Laude, GPA: 94.8/100.
Specialized in business strategy and entrepreneurship, and finance and banking.

2009 *B.Sc. Computer Engineering and Applied Physics, Hebrew University, Jerusalem*
Graduated Magna Cum Laude, GPA: 96.6/100.
Specialized in microelectronics and optoelectronics.

Academic Appointments

7-8/2018 *Visiting Assistant Professor Electrical Engineering*
University of Utah

10/2015-now *Assistant Professor*
Electrical Engineering, Technion
Viterbi fellow at the Technion Computer Engineering Center.

2014-2015 *Post Doctoral Researcher*
Computer Science, Stanford University
Host: Prof. Mark Horowitz.

Professional Experience

2007-2009 *Circuit designer at Intel, Jerusalem.*

Research Interests

VLSI, computer architecture, digital circuits, analog circuits, memory design, hardware for machine learning, neuromorphic computing, cytomorphic computing, system-on-a-chip, FPGA, hardware-software interface, emerging non-volatile memory technologies, EDA, hardware security.

Teaching

Technion

2019-now	*Digital Systems and Computer Organization* (undergraduate level)	Lecturer (in charge)
2018	*Advanced Topics in Computer Engineering* (graduate level, new, with Mark Silberstein and Yoav Etsion)	Lecturer
2017-now	*Seminar in VLSI Systems* (graduate level)	Lecturer
2016-now	*Advanced Circuits and Architectures with Memristor* (undergraduate and graduate level, new)	Lecturer
2015-2018	*Logic Design and Introduction to Computers* (undergraduate level)	Lecturer (in charge)
2015-2016	*Advanced Topics in Computer Design* (graduate level, new)	Lecturer
2011-2014	*Computer Architecture* (undergraduate and graduate level)	Teaching assistant (in charge)
2011-2014	*Advanced VLSI Architectures* (undergraduate and graduate level)	Teaching assistant (in charge)
2009-2013	*Linear Electronics Circuits* (undergraduate level)	Teaching assistant
2009-2014	*SOPC (System on a Programmable Chip) lab* (undergraduate level)	Instructor
2010-2014	*B.Sc. projects, VLSI laboratory* (undergraduate level)	Supervisor

Received commendation as a lecturer (Spring 2018), won six times the Technion excellence award for teaching assistants (Spring 2010, Winter 2011, Spring 2011, Spring 2012, winter 2013, Spring 2014). Supervised the winning projects in the Yehoraz Kasher annual EE project contest in 2011, the Oz Mozes prize in 2012, and the Seiden Prize 2015.

The Hebrew University, Jerusalem.

2009	*Physics Lab for Engineers* (undergraduate level)	Instructor

Professional Service Activities

Technion Activities

2019-now	Technion Hiroshi Fujiwara cyber security research center scientific committee member

Departmental Activities

2019-now	Undergraduate best project committee
2018-now	Graduate studies committee
2016-now	Advanced Circuits Research Center (ACRC) – co-director
2018-now	Undergraduate students' consultant for the VLSI and circuits chain
2015-now	Undergraduate students' consultant for 1st year students
2015-2018	Undergraduate students' consultant for the computer engineering track and the computers chain

Associate Editor

2014-now Microelectronics Journal, Elsevier
2018-now Array, Elsevier

Topic Program Committee Chair
DATE 2020 (topic D14 – Emerging Design Technologies for Future Memories).

Tutorials and Workshops Chair
HPCA 2018.

Program Committee

VLSID 2020, eMTDT 2019, MEMRISYS 2019, SPACE 2019, VLSI-SoC 2019, DATE 2019, APCCAS 2018, VLSI-SoC 2018, MDAC in HiPEAC 2017, 2018, DATE 2018, MemTCAD in HiPEAC 2015, 2016, ChipEx 2016.

PhD Committee

1. Itay Hubara, Technion, 2019.
2. Nimrod Ginzberg, Technion, 2019.
3. Ayal Eshkoli, Technion, 2018.
4. Gil Shomron, Technion, 2018.
5. Binyamin Frankel, Bar Ilan University, 2018.
6. Roman Kaplan, Technion, 2017.
7. Oron Port, Technion, 2017.
8. Robert Gitterman, Bar Ilan University, 2016.
9. Evripides Kyriakides, University of Nicosia, Cyprus, 2016.

MSc Committee

1. Roy Weiss, Technion, 2018.
2. Yuval Ben-Hur, Technion, 2018.
3. Amit Kazimirsky, Bar Ilan University, 2016.
4. Kfir Mizrahi, Technion, 2017.
5. Oren Nishri, Technion, 2017.

Workshop, Tutorials, and Training School Organizer

2018 *Analog Mixed-Signal Circuit Design with Memristors*
Tutorial in ISCAS (Italy)

2017 *Mixed Signal Circuit Design with Memristors*
Tutorial in IEEE COMCAS (Tel Aviv, Israel)

2017 EU COST Action IC-1401
Training school at the Technion (Haifa, Israel)

2017 *Stephen and Sharon Seiden Frontiers in Engineering and Science Workshop: Beyond CMOS: From Devices to Systems*
Workshop (Haifa, Israel)
Co-organizers: Eby Friedman (Rochester) and Avinoam Kolodny (Technion)

2016 *In-Memory and In-Storage Computing with Emerging Technologies*
Workshop in PACT (Haifa, Israel)
Co-organizer: Leonid Yavits (Technion)

Special Session Organizer

2019	*Synthetic Biology – when Biology and Electronics Meet* Co-organizers: Ramez Danial (Technion) and Yosi Shacham-Diamand (Tel Aviv University)	BioCAS
2017	*Memristor for Computing: Myth or Reality?* Co-organizers: Said Hamdioui (TU Delft) and Gert Cauwenberghs (UCSD)	DATE
2016	*Memristors for Computing* Co-organizer: Dietmar Fey (FAU).	CNNA

Scientific Advisory Board

- Chua Memristor Center (CMC) at TU Dresden, Germany.
- International Advisory Board of the 3rd International Conference "Emerging Materials, Technologies and Applications for Non-volatile Memory Devices"

Journal/Conference Referee

1. 17th International Conference on Digital Signal Processing (DSP 2011).
2. 39th International Symposium on Computer Architecture (ISCA 2012).
3. Microelectronics Journal.
4. IEEE Transactions on Nanotechnology.
5. 7th International Symposium on Networks-on-Chip (NOCS 2013).
6. Reed-Muller Workshop (RM 2013).
7. IEEE International Symposium on Circuits and Systems (ISCAS) 2013.
8. Radioengineering.
9. PLOS ONE.
10. IEEE International Symposium on Circuits and Systems (ISCAS) 2014.
11. IEEE Transactions on Electron Devices.
12. Journal of Circuits, Systems, and Computers.
13. IEEE Transactions on Circuits and Systems I: Regular Papers.
14. IEEE Transactions on Circuits and Systems II: Express Briefs.
15. IEEE Transactions on Very Large Scale Integration (VLSI).
16. IEEE Transactions on Neural Networks and Learning Systems.
17. IEEE Journal on Emerging and Selected Topics in Circuits and Systems.
18. International Journal of Electronics and Communications.
19. IEEE Electron Device Letters.
20. Frontiers in Neuroscience.
21. The 48th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO 2015).
22. BIOCAS 2015.
23. IEEE International Symposium on Circuits and Systems (ISCAS) 2016.
24. IEEE Transactions on Computer-Aided Design.
25. IEEE Transactions on Emerging Topics in Computing.
26. ACM Journal on Emerging Technologies in Computing Systems.
27. IET Circuits, Devices, & Systems.
28. International Workshop on Cellular Nanoscale Networks and their Applications (CNNA) 2016.
29. Neural Computing and Applications (NCAA).
30. IEEE International Symposium on Circuits and Systems (ISCAS) 2017.
31. Electronics Letters.
32. High Performance Computer Architecture (HPCA) 2018.
33. IEEE International Symposium on Circuits and Systems (ISCAS) 2018.

34. Nature Nanotechnology.
35. Nature Electronics.
36. Nature Communications.
37. High Performance Computer Architecture (HPCA) 2019.
38. IEEE International Symposium on Circuits and Systems (ISCAS) 2019.
39. IEEE Computer Architecture Letters.
40. IEEE International Conference on Electronics Circuits and Systems 2019.

Grants Referee
1. Israel Science Foundation.

Membership in Professional Societies
IEEE (senior member).

Military Service

1999-2004 *Officer in the IDF, rank: Lieutenant Colonel.*
Participated in several courses and training including sergeant course, officer course, and company commander course and served in several commanding positions including an artillery battery commander and artillery officer course commander.
Currently in the reserve forces.

Fellowships, Awards and Honors

2019	Alexander Goldberg Research Prize Fund (Technion)
2019	**Wolf Foundation Krill Prize for Excellence in Scientific Research**
2018	Commendation as a lecturer (top 12% at the Technion)
2018	KLA-Tencor Excellent Conference Paper Award
2017	**European Research Council starting grant**
2017	**Pazy Memorial Research Award for "the most outstanding and original BSF supported project in mathematical and computer sciences"**
2017	Hershel Rich Technion Innovation Award
2016	Paper selected among top 10 papers in the VLSI-SoC conference to appear in the VLSI-SoC book
2015	Supervised the Seiden Prize for Multidisciplinary Undergraduate Projects in Nano Electronics
2015-2018	Viterbi Fellowship in the Center for Computer Engineering at the Technion
2015	Best Paper of Computer Architecture Letters Award
2015	Supervised the 3rd place winning project in the Yehoraz Kasher Annual EE Project Contest
2015	**IEEE Guillemin-Cauer Best Paper Award**
2015	Viterbi Fellowship for Nurturing Future Faculty Members
2014	Hershel Rich Technion Innovation Award
2014	The Andrew and Erna Finci Viterbi Fellowship
2013, 2014	Vivian Konigsberg Award for Excellence in Teaching (twice)
2013	Sanford Kaplan Prize for Creative Management in High Tech in the 21st Century – 1st place
2013	Best lecturer award – ChipEx 2013

2012	Supervised the winning project in the Oz Mozes Project Contest
2012	Intel award for excellence in research
2011	Vivian Konigsberg Award for Excellence in Teaching (twice)
2011-2014	Hasso Plattner Institute Fellowship (four years)
2011	Irwin and Joan Jacobs Fellowship
2011	Supervised the winning project in the Yehoraz Kasher Annual EE Project Contest
2010, 2012	Sandor Szego Award for Excellence in Teaching (twice)
2010	Benin prize for graduate students
2010	The Marker MBA Case Study Competition finalist
2009	"Peter Brojde Center for Innovative Engineering and Computer Science" excellence final B.Sc. project prize
2007, 2008	Dean's reward for excellence, Hebrew University (twice)
2006-2009	Dean's honorary list, Hebrew University (all four years)

Students Supervised

Completed MSc Theses

2018	Nimrod Wald	*Use of Memristor Based Logic Circuits for Beyond von Neumann Computer Architectures* First employment with Terrain EDA
2018	Ameer Haj Ali	*Performing Image Processing in Memristive Memory Arrays* First employment a PhD student at UC Berkeley
2018	Nishil Talati	*Logic Design for non-von Neumann Architectures using Memristors* First employment a PhD student at University of Michigan
2017	Misbah Ramadan	*Adaptive Programming for Multi-Level Cell ReRAM* Co-advisor Ran Ginosar First employment with Apple
2015	Yifat Levy	*Logic with Memristive Akers Arrays* Co-advisors Avinoam Kolodny and Eby Friedman First employment with Intel

PhD Theses in Progress

2015-2020	Loai Danial	*Neuromorphic Computing with Memristors*
2015-2020	Rotem Ben-Hur	*Logic within the Memory*
2016-2020	Nicolas Wainstein	*RF Front-End Circuits Based on Memristive Devices* Co-advisor: Eilam Yalon
2017-2021	Ben Perach	*Architecture for High Performance Computing and Cyber Security of memristive Memory Processing Unit*
2016-2021	Tzofnat Greenberg-Toledo	*Memristive Artificial Neural Network Accelerator with Online Training*

MSc Theses in Progress

2018-2020	Barak Hoffer	*Chip Design of Memristive Memory Processing Unit*
2018-2020	Adi Eliahu	*PulpFiction – Ultra Low Power Processors with RRAM*
2018-2020	Mor Dahan	*Design of Ferroelectric FET Memories*

Post-Docs

2019-now	Kunal Korgaonkar	
2017-2018	John Reuben	First employment Associate Professor in Vellore Institute of Technology, India)

Sponsored Long-Term Visitors

June 2019-now	Rajaie Ismeeh	Visiting scholar *Bir Zeit University, Ramallah, Palestinian Territories*
May-July 2019	Anmol Jain	Visiting scholar *Indian Institute of Technology, Roorkee, India*
May 2019-now	Jeffrey Louis	Visiting scholar *BITS Pilani, India*
May 2019-now	Shivansh Dwivedi	Visiting scholar *Indian Institute of Technology, Indore, India*
May 2019-now	Kanishka Sharma	Visiting scholar *Indian Institute of Technology, Indore, India*
October 2018-May 2019	Varun Tandon	Visiting scholar
July-September 2018	Debjyoti Bhattacharjee	Visiting scholar *Nanyang Technological University, Singapore*
June 2018-May 2019	Kunal Korgaonkar	Visiting scholar *University of California, San Diego*
May-July 2018	Vasu Gupta	Visiting scholar *BITS Pilani, India*
May-July 2018	Sidharth Thomas	Visiting scholar *Indian Institute of Technology, Roorkee, India*
May-July 2018	Keshav Tiwari	Visiting scholar *Indian Institute of Technology, Roorkee, India*
December 2016-January 2017	Elias Cohen	Visiting scholar *Reed College, Oregon*
May-July 2016	Nishil Talati	Visiting scholar *BITS Pilani, India*

B.Sc. Projects

1. Dmitry Belousov and Slavik Liman, "Memristor-based Circuits" (*Winners of the Yehoraz Kasher EE Project Contest*).
2. Zahi Lahti and Elad Osherov, "Memristor Model."
3. Oren Lev and Emanuel Darji, "Analysis of Power Grids."

4. Keren Talisveyberg and Dmitry Fliter, "Memristor Verilog-A and MATLAB Modeling."
5. Ilan Shusterman and Michael Rozenblat, "Memristor-based Memory Analysis."
6. Leon Karbachevsky and Boaz Blankrot, "Memristor-based Analog Circuits."
7. Guy Satat and Nimrod Wald, "Memristor-based Full Adder," "Memristor-based Multithreading Processor" (*Winners of the Oz Mozes Project Contest*).
8. Boris Bashkansky and Lahav Madlinsky, "Memristor-based Memory Array Circuit and Layout Design."
9. Rotem Tabach and Dina Leshinsky, "Neuromorphic Systems."
10. Yiffah Fishler and Shir Lindenbaum, "Memristor Modeling."
11. Firas Shama and Louie Matar, "Memristor-based Multithreading Processor."
12. Keren Tendeter and Shiran Shuster, "Simulator for Memristor-based Memory."
13. Misbah Ramadan and Loai Danial, "Analysis of a Memristor-based Crossbar."
14. Hani Bezalel and Rotem Gabay, "Controller for Memristor-based Logic."
15. Benny Fellman and Gilad Tsoran, "Memristor-based Multithreading Processor."
16. Moab Arar and Muhammad Grefat, "Simulation Tools for Emerging Memory Technologies."
17. Israel Goldstein and Alex Dozortzev, "Memristor-based Crossbar for Neural Networks."
18. Misbah Ramadan, "Memristor Modeling."
19. Yoav Furman and Rula Naffaa, "Complementary MRL."
20. Avishay Drori and Elad Amrani, "Logic Design with Memristive Devices."
21. Eyal Rosenthal and Sergey Greshnikov, "Machine Learning with Memristors."
22. Itay Tsabari, "DNA Sequencing by Logic within Memory."
23. Adi Eliahu, "PulpFiction."
24. Barak Hoffer, "Testing of Memristive Memory Processing Unit."

Research Grants (Total Funding 2015-2019: $4,140,000)

Competitive

2019-2020 *KAMIN - Israel Innovation Authority* Project no. 66769
Memristor-Based Reconfigurable RF Circuits
(437K NIS for 1 years)

2019-2020 *Technion Hiroshi Fujiwara cyber security research center and the Israel cyber bureau*
(140K NIS for 1 year)

2018-2020 *MAGNET consortium - GenPro - Israel Innovation Authority*
(350K NIS for 18 months)

2018-2020 *Technion Hiroshi Fujiwara cyber security research center and the Israel cyber bureau*
Co-PI: Avi Mendelson (Technion)
(300K NIS for 3 years)

2018-2019 *Julia and Joshua Ruch Exchange Program*
Co-PI: Zhiru Zhang (Cornell)
($7K for traveling)

2017-2022 ***European Research Council Starting Grant*** Grant no. 757259
Memristive In-Memory Processing Systems
(1.5M Euro for 5 years)

2017-2021 *Israel Science Foundation (ISF)* Grant no. 1514/17
Design of Computer Memories with Independent Computing Capabilities
(1M NIS for 4 years)

2017-2020 *Ministry of Science and Technology*
Integrated Genetics and Memristors breaking through the scaling limits of Moore's law
Co-PI: Ramez Daniel (Technion)
(1.555M NIS for 3 years)

2017-2019 *US–Israel Binational Science Foundation (BSF)* Grant no. 2016016
High-Performance Normally-Off Parallel Processing
Co-PI: Pierre-Emmanuel Gaillardon (University of Utah)
($150K for 3 years)

2017-2019 *NSF-BSF* Grant no. 2015709
Dynamically Configurable Memory Technology Based on Ferroelectric-Gated FET's (FeFET's)
Co-PIs: Moshe Eizenberg (Technion) and Ma Tso-Ping (Yale University)
($150K for 3 years)

2017-2018 *Russell Berrie Nanotechnology Institute Nevet*
Integrated Genetics and Nanoelectronics Breaking through the Scaling Limits of Moore's Law
Co-PI: Ramez Daniel (Technion)
($40K for 1 year)

2017 *Israel Science Foundation equipment grant for new faculty* Grant no. 1515/17
(758,517 NIS)

2016-2018 *KAMIN - Israel Innovation Authority* Project no. 57681
Analog to Digital Converters with Memristive Neural Network
(840K NIS for 2 years)

2016-2019 *MAGNET consortium - HiPER - Israel Innovation Authority*
(700K NIS for 3 years)

2015-2018 ICT COST action
Memristors – Devices, Models, Circuits, Systems and Applications (MemoCIS)
(travel grants)

Industrial

2018-2019 *Huawei*
($200K for 1 years)

2017 *Cisco University Research Program Fund*
Vulnerability Analysis of Emerging Nonvolatile Memory Technologies
Co-PI: Avi Mendelson (Technion)
($80K for 1 years)

2015-2017 *Intel Collaborative Research Institute – Computational Intelligence*
Memory Intensive Architectures
($137.5K for 2 years)

PUBLICATIONS (students are underlined)

Thesis

S. Kvatinsky, "Memristor-Based Circuits and Architectures," PhD dissertation, August 2014.

Refereed Journal Papers:

1. **S. Kvatinsky**, E. G. Friedman, A. Kolodny, and U. C. Weiser, "TEAM - ThrEshold Adaptive Memristor Model," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 60, No. 1, pp. 211-221, January 2013. ***2015 IEEE Guillemin-Cauer Best Paper Award.***
2. **S. Kvatinsky**, E. G. Friedman, A. Kolodny, and U. C. Weiser, "The Desired Memristor for Circuit Designers," *IEEE Circuits and Systems Magazine*, Vol. 13, No. 2, pp. 17-22, second quarter 2013.
3. **S. Kvatinsky**, Y. H. Nacson, Y. Etsion, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Memristor-Based Multithreading," *IEEE Computer Architecture Letters*, Vol. 13, No. 1, pp. 41-44, January-June 2014.
4. **S. Kvatinsky**, N. Wald, G. Satat, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Memristor-Based Material Implication (IMPLY) Logic: Design Principles and Methodologies," *IEEE Transactions on Very Large Scale Integration (VLSI)*, Vol. 22, No. 10, pp. 2054-2066, October 2014.
5. **S. Kvatinsky**, D. Belousov, S. Liman, G. Satat, N. Wald, E. G. Friedman, A. Kolodny, and U. C. Weiser, "MAGIC – Memristor Aided LoGIC," *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 61, No. 11, pp. 895-899, November 2014.
6. Y. Levy, J. Bruck, Y. Cassuto, E. G. Friedman, A. Kolodny, E. Yaacobi, and **S. Kvatinsky**, "Logic Operation in Memory Using a Memristive Akers Array," *Microelectronics Journal*, Vol. 45, No. 11, pp. 1429-1437, November 2014.
7. **S. Kvatinsky**, M. Ramadan, E. G. Friedman, and A. Kolodny, "VTEAM – A General Model for Voltage Controlled Memristor," *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 62, No. 8, pp. 786-790, August 2015.
8. R. Patel, **S. Kvatinsky**, E. G. Friedman, and A. Kolodny, "Multistate Register Based on Resistive RAM," *IEEE Transactions on Very Large Scale Integration (VLSI)*, Vol. 23, No. 9, pp. 1750-1759, September 2015.
9. D. Soudry, D. Di Castro, A. Gal, A. Kolodny, and **S. Kvatinsky**, "Memristor-based Multilayer Neural Networks with Online Gradient Descent Training," *IEEE Transactions on Neural Networks and Learning Systems*, Vol. 26, No. 10, pp. 2408-2421, October 2015.
10. L. Yavits, **S. Kvatinsky**, A. Morad, and R. Ginosar, "Resistive Associative Processor," *IEEE Computer Architecture Letters*, Vol. 14, No. 2, July-December 2015. ***Best of CAL winner 2015***.
11. A. Morad, L. Yavits, **S. Kvatinsky**, and R. Ginosar, "Resistive GP-SIMD Processing In-Memory," *ACM Transactions on Architecture and Code Optimization*, Vol. 12, No. 4, Article 57, January 2016.
12. N. Talati, S. Gupta, P. Mane, and **S. Kvatinsky**, "Logic Design within Memristive Memories Using Memristor Aided loGIC (MAGIC)," *IEEE Transactions on Nanotechnology*, Vol. 15, No. 4, pp. 635-650, July 2016.
13. Y. Cassuto, **S. Kvatinsky**, and E. Yaakobi, "Information-Theoretic Sneak Path Mitigation in Memristor Crossbar Arrays," *IEEE Transactions on Information Theory*, Vol. 62, No. 9, pp. 4801-4814, September 2016.
14. A. Pedram, S. Richardson, S. Galal, **S. Kvatinsky**, and M. Horowitz, "Dark Memory and Accelerator-Rich System Optimization in the Dark Silicon Era", *IEEE Design and Test*, Vol. 34, No. 2, pp. 39-50, April 2017.
15. A. Doz, I. Goldstein, and **S. Kvatinsky**, "Analysis of the Row Grounding Method in a Memristor-Based Crossbar Array," *International Journal of Circuit Theory and Applications*, Vol. 46, No. 1, pp. 122-137, January 2018.

16. L. Danial, N. Wainstein, S. Kraus, and **S. Kvatinsky**, "DIDACTIC: A Deeply Intelligent Digital-to-Analog Converter with a Trainable Integrated Circuit using Memristors," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, Vol. 8, No. 1, pp. 146-158, March 2018.
17. N. Wainstein and **S. Kvatinsky**, "TIME – Tunable Inductors using MEmristors," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 65, No. 5, pp. 1505-1515, May 2018.
18. A. Haj Ali, R. Ben Hur, N. Wald, R. Ronen, and **S. Kvatinsky**, "Not in Name Alone: A Memristive Memory Processing Unit for Real In-Memory Processing," *IEEE Micro*, Vol. 38, No. 5, pp. 13-21, September/October 2018.
19. N. Wainstein and **S. Kvatinsky**, "A Lumped RF Model for Nanoscale Memristive Devices and Non-Volatile Single-Pole Double-Throw Switches," *IEEE Transactions on Nanotechnology*, Vol. 17, No. 5, pp. 873-883, September 2018.
20. L. Danial, N. Wainstein, S. Kraus, and **S. Kvatinsky**, "Breaking Through the Speed-Power-Accuracy Tradeoff in ADCs using a Memristive Neuromorphic Architecture," *IEEE Transactions on Emerging Topics in Computational Intelligence*, Vol. 2, No.5, pp. 396-409, October 2018.
21. A. Haj Ali, R. Ben-Hur, N. Wald, R. Ronen, and **S. Kvatinsky**, "IMAGING - In-Memory AlGorithms for Image ProcessiNG," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 65, No. 12, pp. 4258-4271, December 2018.
22. N. Talati, H. Ha, B. Perach, R. Ronen, and **S. Kvatinsky**, "CONCEPT: A Column Oriented Memory Controller for Efficient Memory and PIM Operations in RRAM," *IEEE Micro*, Vol/ 39, No. 1, pp. 33-43, January/February 2019.
23. E. Giacomin, T. Greenberg-Toledo, **S. Kvatinsky**, and P.-E. Gaillardon, "A Robust Digital RRAM-based Convolutional Block for Low-Power Image Processing and Learning Applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 62, No. 2, pp. 643-654, February 2019.
24. T. Greenberg-Toledo, R. Mazor, A. Haj Ali, and **S. Kvatinsky**, "Supporting the Momentum Algorithm Using a Memristor-Based Synapse," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 66, No. 4, pp. 1571-1583, April 2019.
25. N. Wald and **S. Kvatinsky**, "Influence of Parameter Variations and Environment for Real Processing-In-Memory using Memristor Aided Logic (MAGIC)," *Microelectronics Journal*, Vol. 86, pp. 22-33, April 2019.
26. M. Ramadan, N. Wainstein, R. Ginosar, and **S. Kvatinsky**, "Adaptive Programming in Multi-Level Cell ReRAM," *Microelectronics Journal*, Vol. 90, pp. 169-180, August 2019.
27. B. Perach and **S. Kvatinsky**, "An Asynchronous and Low-Power True Random Number Generator using STT-MTJ," *IEEE Transactions on Very Large Scale Integration Systems*, (in press).
28. R. Ben-Hur, R. Ronen, A. Haj-Ali, D. Bhattacharjee, A. Eliahu, N. Peled, and **S. Kvatinsky**, "SIMPLER MAGIC: Synthesis and Mapping of In-Memory Logic Executed in a Single Row to Improve Throughput," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, (in press).

Submitted Refereed Journal Papers:

29. L. Danial, E. Pikhay, E. Herbelin, N. Wainstein, V. Gupta, N. Wald, Y. Roizin, R. Daniel, and **S. Kvatinsky**, "A Two-Terminal Floating-Gate Memristive Device for Analog Neuromorphic Systems," (in review).
30. K. Korgaonkar, R. Ronen, A. Chattopadhyay, and **S. Kvatinsky**, "Bitlet Model: Understanding the Sweet Spots and Limits of Processing in Memory," (in review).
31. T. Greenberg-Toledo, B. Perach, D. Soudry, and **S. Kvatinsky**, "MTJ-Based Hardware Synapse Design for Ternary Deep Neural Networks," (in review).

32. N. Wainstein, E. Yalon, G. Adam, and S. Kvatinsky, "High-Performance Radiofrequency Switches Based on Resistive Memory Technologies – A Survey ", (in review).

Book Chapters:

1. N. Wald, E. Amrany, A. Drory, and **S. Kvatinsky**, "Logic with Unipolar Memristors: Circuits and Design Methodology," *VLSI-SoC: System-on-Chip in the Nanoscale Era – Design, Verification and Reliability*, IFIP Advances in Information and Communication Technology, T. Hollstein, J. Raik, S. Kostin, A. Tšertov, I. O'Connor, R. Reis (Eds.), Springer, Vol. 508, Chapter 2, pp. 24-40, 2017.
2. N. Talati, R. Ben-Hur, N. Wald, A. Haj Ali, J. Reuben, and **S. Kvatinsky**, "mMPU – A Real Processing-in-Memory Architecture to Combat the von Neumann Bottleneck," *Applications of Emerging Memory Technology*, The Springer Series in Advanced Microelectronics, M. Suri (Ed.), Springer, Chapter 8, pp. 191-213, 2020.
3. J. Reuben, R. Ben Hur, N. Wald, N. Talati, A. Haj Ali, P.-E. Gaillardon, and **S. Kvatinsky**, "A Taxonomy and Evaluation Framework for Memristive Logic," *Handbook of Memristor Networks*, Springer (in press).
4. A. Haj Ali, R. Ronen, R. Ben-Hur, N. Wald, and **S. Kvatinsky**, "Memristor-Based Processing-in-Memory and its Application on Image Processing," *Memristive Devices for Brain-Inspired Computing*, Elsevier (in press).

Refereed Conference Papers:

1. **S. Kvatinsky**, E. G. Friedman, A. Kolodny, and L. Schächter, "Power Grid Analysis Based on a Macro Circuits Model", *Proceedings of the IEEE Convention of Electrical and Electronics Engineers in Israel*, pp. 708-712, November 2010.
2. **S. Kvatinsky**, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Memristor-based IMPLY Logic Design Flow," *Proceedings of the IEEE International Conference on Computer Design*, pp.142-147, October 2011.
3. **S. Kvatinsky**, N. Wald, G. Satat, E. G. Friedman, A. Kolodny, and U. C. Weiser, "MRL – Memristor Ratioed Logic," *Proceedings of the International Cellular Nanoscale Networks and their Applications*, pp. 1-6, August 2012.
4. **S. Kvatinsky**, K. Talisveyberg, D. Fliter, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Models of Memristors for SPICE Simulations," *Proceedings of the IEEE Convention of Electrical and Electronics Engineers in Israel*, pp. 1-5, November 2012.
5. Y. Cassuto, **S. Kvatinsky**, and E. Yaakobi, "Sneak-Path Constraints in Memristor Crossbar Arrays," *Proceeding of the Annual Non-Volatile Memories Workshop*, March 2013.
6. Y. Cassuto, **S. Kvatinsky**, and E. Yaakobi, "Sneak-Path Constraints in Memristor Crossbar Arrays," *Proceedings of the IEEE International Symposium on Information Theory*, pp. 156-160, July 2013.
7. **S. Kvatinsky**, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Memory Intensive Computing," *Proceeding of the Annual Non-Volatile Memories Workshop*, March 2014.
8. Y. Cassuto, **S. Kvatinsky**, and E. Yaakobi, "On the Channel Induced by Sneak-Path Errors in Memristor Arrays," *Proceedings of the International Conference on Signal Processing and Communication*, pp. 1-6, July 2014.
9. **S. Kvatinsky**, Y. H. Nacson, R. Patel, Y. Etsion, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Memristive Multistate Pipeline Register," *Proceedings of the International Cellular Nanoscale Networks and their Applications*, pp. 1-2, July 2014.
10. Z. Jiang, P. Huang, L. Zhao, **S. Kvatinsky**, S. Yu, X. Liu, J. Kang, Y. Nishi, and H.-S. P. Wong, "Analysis and Predication on Resistive Random Access Memory (RRAM) 1S1R Array," *Proceedings of the 2015 International Memory Workshop*, pp. 1-4, May 2015.
11. R. Ben-Hur and **S. Kvatinsky**, "Processing within a Memristive Memory," *Proceedings of the Workshop on Memristor Technology, Design, Automation and Computing*, January 2016.

12. L. Danial and **S. Kvatinsky**, "Memristive Artificial Neural Networks Based Analog to Digital Converter (ADC)," *Proceedings of the Workshop on Memristor Technology, Design, Automation and Computing*, January 2016.
13. M. Ramadan, **S. Kvatinsky**, and R. Ginosar, "Memristor Modeling," *Proceedings of the Workshop on Memristor Technology, Design, Automation and Computing*, January 2016.
14. E. Rosenthal, S. Greshnikov, D. Soudry, and **S. Kvatinsky**, "A Fully Analog Memristor-Based Multilayer Neural Network with Online Backpropagation Training," *Proceeding of the IEEE International Symposium on Circuits and Systems*, pp. 1394-1397, May 2016.
15. Y. Cassuto, **S. Kvatinsky**, and E. Yaakobi, "Write Sneak-Path Constraints Avoiding Disturbs in Memristor Crossbar Arrays," *Proceedings of the IEEE International Symposium on Information Theory*, pp. 950-954, July 2016.
16. R. Ben-Hur and **S. Kvatinsky**, "Memory Processing Unit for In-Memory Processing," *Proceedings of the IEEE/ACM International Symposium on Nanoscale Architectures*, pp. 171-172, July 2016.
17. R. Ben-Hur, N. Talati, and **S. Kvatinsky**, "Algorithmic Considerations in Memristive Memory Processing Units (MPU)," *Proceedings of the International Cellular Nanoscale Networks and their Applications*, pp. 1-2, August 2016.
18. E. Amrany, A. Drory, and **S. Kvatinsky**, "Logic Design with Unipolar Memristors," *Proceedings of the IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, pp. 1-5, September 2016. ***Selected for post-conference book (top 10 papers).***
19. A. Vasilyev, N. Bhagdikar, S. Richardson, A. Pedram, **S. Kvatinsky**, and M. Horowitz, "Evaluating Programmable Architectures for Image and Vision Applications," *Proceedings of the Annual ACM/IEEE International Symposium on Microarchitecture*, pp. 1-13, October 2016.
20. H. Ha, A. Pedram, S. Richardson, **S. Kvatinsky**, and M. Horowitz, "Improving Energy Efficiency of DRAM by Exploiting Half Page Row Access," *Proceedings of the Annual ACM/IEEE International Symposium on Microarchitecture*, pp. 1-12, October 2016.
21. R. Ben-Hur and **S. Kvatinsky**, "Memristive Memory Processing Unit (MPU) Controller for In-Memory Processing", *Proceedings of the IEEE International Conference on Science of Electrical Engineering*, pp. 1-5, November 2016.
22. N. Wald and **S. Kvatinsky**, "Design Methodology for Stateful Memristive Logic Gates", *Proceedings of the IEEE International Conference on Science of Electrical Engineering*, pp. 1-5, November 2016.
23. S. Hamdioui, **S. Kvatinsky**, G. Cauwenberghs, L. Xie, K. Bertels, N. Wald, S. Joshi, H. M. Elsayed, and H. Corporaal, "Memristor for Computing: Myth or Reality?" *Proceedings of the Design, Automation and Test in Europe*, pp. 722-731, March 2017.
24. **S. Kvatinsky**, R. Ben-Hur, N. Talati, and N. Wald, "mMPU: Memristive Memory Processing Unit," *International Conference on Memristive Materials, Devices & Systems*, April 2017.
25. L. Azriel and **S. Kvatinsky**, "Towards a Memristive Hardware Secure Hash Function (MemHash)", *Proceedings of the IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, pp. 51-55, May 2017.
26. N. Talati, Z. Wang, and **S. Kvatinsky,** "Rate-Compatible and High-Throughput Architecture Designs for Encoding LDPC Codes," *Proceeding of the IEEE International Symposium on Circuits and Systems*, pp. 1-4, May 2017.
27. N. Wainsten and **S. Kvatinsky**, "An RF Memristor Model and Memristive Single-Pole Double Throw Switches," *Proceeding of the IEEE International Symposium on Circuits and Systems*, pp. 1-4, May 2017.
28. J. Reuben, R. Ben Hur, N. Wald, N. Talati, A. Haj Ali, P.-E. Gaillardon, and **S. Kvatinsky**, "Memristive Logic: A Framework for Evaluation and Comparison," *Proceeding of the IEEE International Symposium on Power and Timing Modeling, Optimization and Simulation*, pp. 1-8, September 2017.

29. H. Abo Hanna, L. Danial, **S. Kvatinsky,** and R. Daniel, "Modeling Biochemical Reactions and Gene Networks with Memristors," *Proceeding of the IEEE Symposium on Biological Circuits and Systems*, pp. 1-4, October 2017.
30. R. Ben Hur, N. Wald, N. Talati, and **S. Kvatinsky**, "SIMPLE MAGIC: Synthesis and Mapping of Boolean Functions for Memristor Aided Logic (MAGIC)," *Proceeding of the IEEE International Conference on Computer Aided Design*, pp. 225-232, November 2017. ***KLA-Tencor Excellent Conference Paper Award.***
31. N. Talati, A. Haj Ali, R. Ben Hur, N. Wald, R. Ronen, P.-E. Gaillardon, and **S. Kvatinsky**, "Practical Challenges in Delivering the Promises of Real Processing-in-Memory Machines," *Proceedings of the Design Automation and Test in Europe*, pp. 1628-1633, March 2018.
32. A. Haj Ali, R. Ben-Hur, N. Wald, and **S. Kvatinsky**, "Efficient Algorithms for In-Memory Fixed Point Multiplication Using MAGIC," *Proceeding of the IEEE International Symposium on Circuits and Systems*, pp. 1-5, May 2018.
33. G. C. Adam, R. Badulescu, S. Iordanescu, N. Wainstein, and **S. Kvatinsky**, "A TiO_2 – Based Radio Frequency Resistive Switch," *Proceedings of the International Conference on Electron, Ion, and Photon Beam Technology and Nanofabrication*, June 2018.
34. L. Danial and **S. Kvatinsky**, "Real-Time Trainable Data Converters for General Purpose Applications," *Proceeding of the IEEE/ACM International Symposium on Nanoscale Architectures*, July 2018.
35. H. Abo Hanna, L. Danial, **S. Kvatinsky,** and R. Daniel, "Memristors as Artificial Biochemical Reactions in Cytomorphic Systems," *Proceedings of the IEEE International Conference on Science of Electrical Engineering*, December 2018.
36. B. Perach and **S. Kvatinsky**, "STT-ANGIE: Asynchronous True Random GEnerator Using STT-MTJ," *Proceedings of the Design, Automation and Test in Europe*, March 2019.
37. L. Danial, S. Thomas, and **S. Kvatinsky**, "Delta-Sigma Modulation Neurons for High-Precision Training of Memristive Synapses in Deep Neural Networks," *Proceedings of the International Symposium on Circuits and Architectures*, pp. 1-5, May 2019.
38. N. Wainstain, T. Tsabari, Y. Goldin, E. Yalon, and **S. Kvatinsky**, "A Dual-Band CMOS Low-Noise Amplifier using Memristor-Based Tunable Inductors," *Proceedings of the IEEE Computer Society Annual Symposium on VLSI*, July 2019 (in press).
39. M. Ottavi, V. Gupta, S. Khandelwal**, S. Kvatinsky**, J. Mathew, E. Martinelli, and A. Jabir, "The Missing Applications Found: Robust Design Techniques and Novel Uses of Memristors," *Proceedings of IEEE International Symposium on On-Line Testing and Robust System Design*, July 2019 (in press).
40. **S. Kvatinsky**, "Real Processing-in-Memory with Memristive Memory Processing Unit (mMPU)," *Proceeding of the IEEE International Conference on Application-Specific Systems, Architectures and Processors*, July 2019 (in press).
41. J. Vieira, E. Giacomin, Y. Qureshi, M. Zapater, X. Tang, **S. Kvatinsky**, D. Atienza, and P.-E. Gaillardon, "A Product Engine for Energy Efficient Execution of Binary Neural Networks Using Resistive Memories," *Proceedings of the IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, October 2019 (in press).

Submitted Refereed Conference Papers:

42. L. Danial, K. Sharma, S. Dwivedi, and **S. Kvatinsky**, "Logarithmic Neural Network Data Converters using Memristors for Biomedical Applications," (submitted).
43. A. Eliahu, R. Ronen, P.-E. Gaillardon, and **S. Kvatinsky**, "multiPULPly: A Multiplication Engine for Accelerating Neural Networks on Ultra-Low-Power Architectures, (submitted).

Magazines:

1. R. Daniel and **S. Kvatinsky**, "Combining Biology and Electronics Using Emerging Memristive Technologies," *Tower Jazz Technical Journal*, Vol. 8, pp. 30-38, June 2017.

Technical Reports:

1. R. Ben Hur, N. Wald, N. Talati, and **S. Kvatinsky**, " Latency Optimized Mapping of Logic Functions for Memristor Aided Logic (MAGIC)," *CCIT Technical Report #908*, December 2016.
2. X. Yang, J. Pu, B. B. Rister, N. Bhagdikar, J. Ragan-Kelley, S. Richardson, **S. Kvatinsky**, A. Pedram, and M. Horowitz, "A Systematic Approach to Blocking Convolutional Neural Networks," *ArXiv:1606.04209*, June 2016.
3. **S. Kvatinsky**, M. Ramadan, E. G. Friedman, and A. Kolodny, "VTEAM - A General Model for Voltage Controlled Memristors," *CCIT Technical Report #*856, April 2014.
4. D. Soudry, D. Di Castro, A. Gal, A. Kolodny, and **S. Kvatinsky**, "Hebbian Learning Rules with Memristors," *CCIT Technical Report #*840, September 2013.
5. **S. Kvatinsky**, E. G. Friedman, A. Kolodny, and U. C. Weiser, "TEAM - ThrEshold Adaptive Memristor Model," *CCIT Technical Report #80*4, January 2012.
6. **S. Kvatinsky**, K. Talisveyberg, D. Fliter, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Verilog-A for Memristor Models," *CCIT Technical Report #801*, December 2011.
7. **S. Kvatinsky**, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Memristor-based IMPLY Logic Design Flow," *CCIT Technical Report #795*, August 2011.

Patents Granted:

1. S. Kvatinsky, Y. Levy, and A. Kolodny, "Memristive Akers Logic Array," US patent no. 9548741.
2. A. Kolodny, S. Kvatinsky, R. Patel, and E. G. Friedman, "Multistate Register Having a Flip Flop and Multiple Memristive Devices," US patent no. 9679650 B2.
3. S. Kvatinsky, D. Belousov, S. Liman, N. Wald, and G. Satat, "A Pure Memristive Logic Gate," US patent no. 9685954.
4. D. Soudry, S. Kvatinsky, A. Gal, D. Di Castro, and A. Kolodny, "Implementating multiplication in adaptive circuits using memristive devices," US patent no. 9754203.
5. S. Kvatinsky, D. Belousov, S. Liman, N. Wald, and G. Satat, "Pure Memristive Logic Gate," US patent no. 10284203.
6. M. Ramadan, S. Kvatinsky, and R. Ginosar, "Adaptive Programming for Memories with Multi-Level Cells," US patent application no. 62/432,615.

Patents Filed:

7. S. Kvatinsky, A. Kolodny, and U. C. Weiser, "Memristor-Based Multithreading," Israel patent application no. 225988.
8. S. Kvatinsky, A. Kolodny, and U. C. Weiser, "Memristor-Based Multithreading," US patent application no. 14/219,030.
9. A. Morad, L. Yavits, S. Kvatinsky, and R. Ginosar, "Hybrid Processor," US patent application no. 14/979,880.
10. A. Drori, E. Amrani, and S. Kvatinsky, "Implementation of Logic Circuits with Unipolar Memristive Devices, Thin Film Resistive Switches, and Phase Change Memory," US patent application no. 62/340,559.
11. L. Azriel and S. Kvatinsky, "Memristive Security Hash Function," US patent application no. 15/965,924.
12. L. Danial and S. Kvatinsky, "Analog to Digital Converter using Memristors in a Neural Network," US patent application no. 62/585,578.
13. L. Danial and S. Kvatinsky, "Reconfigurable DAC Implemented by Memristor Based Neural Network," US patent application no. 62/530,920.

14. B. Perach and S. Kvatinsky, "Asynchronous True Random Number Generator using STT-MTJ." US patent application no. 62/774,258.
15. T. Greenberg-Toledo, D. Soudry, and S. Kvatinsky, "MTJ-Based Hardware Synapse Implementation for Ternary and Binary Deep Neural Networks," US patent application no. 62/730,554.
16. L. Danial and S. Kvatinsky, "Delta-Sigma Modulation Neurons for High Precision Training of Memristive Synapses in Deep Neural Networks," US patent application no. 62/774,933.
17. P.-E. Gaillardon, E. Giacomin, and S. Kvatinsky, "A Robust Digital RRAM-based Convolutional Block for Low-Power Image Processing and Learning Applications," US patent application no. 62/734,023.

Selected Talks (Plenary, Keynote, and Invited)

Real Processing-in-Memory using Memristive Memory Processing Unit

- International Conference on Memristive Materials, Devices and Systems, Dresden, Germany, July 2019 (keynote).
- IEEE International Symposium on Online Testing and Robust System Design, Rhodes, Greece, July 2019 (invited).
- IEEE International Conference on the Science of Electrical Engineering, Eilat, Israel, December 2018 (invited).
- In-Memory Computing: Emerging Devices, Architectures, and Applications, Politecnico di Torino, Italy, September 2018 (invited).
- 18th International Forum on MPSoC for Software Defined Hardware, Snowbird, UT, USA, August 2018 (plenary talk).
- International Conference on Neuromorphic Systems, Knoxville, Tennessee, USA, July 2018 (invited).
- The 8th Workshop on Systems for Multi-core and Heterogeneous Architectures, Porto, Portugal, April 2018 (keynote).
- Emertech 2018, Singapore, April 2018 (invited).

A Taxonomy and Evaluation Framework to Memristive Logic

- MemoCIS workshop, Dresden, Germany, September 2018 (plenary talk).

Logic Synthesis and Automation for Memristive Memory Processing Unit

- EPFL Workshop on Logic Synthesis and Emerging Technologies, Lausanne, Switzerland, September 2017 (invited).

Memristors for Learning

- IEEE International Conference on Science of Electrical Engineering, November 2016 (invited).

Computation with Memristors

- MemoCIS workshop, Palma de Mallorca, Spain, September 2016 (invited).

Introduction to Memristors

- ChipEx 2016, Tel Aviv, May 2016 (invited).

Avoiding the Dark Ages with Memristors

- MemoCIS Workshop: “Memristors: at the Crossroad of Devices and Applications”, Milan, March 2016 (keynote).

Emerging Memory Technologies: Challenges and Opportunities

- DesignEx 2015, Tel Aviv, November 2015 (invited).

Additional Selected Talks

Memristors for Artificial Intelligence

- Bar Ilan University, Ramat Gan, Israel, April 2019 (department colloquium).
- Samsung, Ramat Gan, Israel, April 2019.

Designing Extremely Efficient Computers with Memristors

- University of California, Irvine, CA, August 2018.
- University of Utah, Salt Lake City, Utah, July 2018.

Memristors: The Future of Non-Volatile Memory or Perhaps Even More?

- Intel, Jerusalem, Israel, January 2019.
- Applied Physics, School of Computer Engineering and Science, Hebrew University, Jerusalem, May 2018 (department colloquium).
- Department of Material Engineering and Science, Technion – Israel Institute of Technology, May 2018 (department colloquium).

Real Processing-in-Memory using Memristive Memory Processing Unit

- Universita' della Tuscia, Viterbo, Italy, March 2018.
- University of Rome Tor Vergata, Italy, March 2018.

Artificial Intelligence: Can a Computer Outsmart Humans?

- Italy-Technion Society event, Rome, Italy, March 2018 (invited).

A Taxonomy and Evaluation Framework to Memristive Logic

- MDAC HiPEAC, Manchester, United Kingdom, January 2018.

Memory Intensive Architectures

- Intel, Hillsborough, OR, USA, June 2017.

mMPU: Memristor Memory Processing Unit

- 2017 Stephen and Sharon Seiden Frontiers in Engineering and Science Workshop: Beyond CMOS: From Devices to Systems, Technion, Haifa, Israel, June 2017.
- Intel Collaborative Research Institute - Computational Intelligence Retreat, Haifa, Israel May 2017.

Computation with Memristors

- Intel, Haifa, Israel, December 2016.

Designing Extremely Energy Efficient Computers with Memristors

- 3rd Green Photonics Symposium, Technion, Haifa, Israel, March 2016.
- UT Dresden, Dresden, Germany, February 2016.
- Qualcomm, Haifa, Israel, January 2016.
- Mellanox, Yokneham, Israel, December 2015.
- Marvell, Petach Tikva, Israel, November 2015.
- Qualcomm, San Diego, July 2015.
- ARM, San Jose, CA, June 2015.
- UCLA, Los Angeles, CA, June 2015.
- UC Santa Barbara, Santa Barbara, CA, June 2015.

- Nvidia Research, Santa Clara, CA, May 2015.
- Intel Labs, Hillsborough, OR, May 2015.

Designing Extremely Energy Efficient Computers

- UT Austin, Austin, TX, March 2015.
- Technion – Israel Institute of Technology, Haifa, Israel, January 2015.
- Hebrew University of Jerusalem, Jerusalem, Israel, January 2015.
- Ben Gurion University of the Negev, Beer Sheva, Israel, January 2015.

Memory Intensive Computing

- Tel Aviv University, Tel Aviv, July 2014.
- *DATE 2014*, Dresden, Germany, March 2014.
- *HiPEAC 2014*, Vienna, Austria, January 2014.

Building the Computers of the Future – a Talk about Resistors, Memories, and More

- *Jacobs Showcase Lecture Series: Much is New Under the Sun*, Technion - Israel Institute of Technology, Haifa, Israel, November 2013.

Memristors – Not Only Memory

- Princeton University, NJ, September 2013.
- Columbia University, NY, September 2013.
- Stanford University, Stanford, CA, September 2013.
- UC Berkeley, Berkeley, CA, September 2013.
- HP Labs, Palo Alto, CA, September 2013.
- UC San Diego, La Jolle, CA, September 2013.
- UC Santa Barbara, Santa Barbara, CA, October 2013.
- *The International Conference of the Israeli Semiconductor Industry (ChipEx 2013)*, Tel Aviv, Israel, May 2013. **Best lecture award**.

The Desired Memristor for Circuit Designers

- *Nature Conference on "Frontiers in Electronic Materials: Correlation Effects and Memristive Phenomena*," Aachen, Germany, June 2012.

Memristor-based Logic Circuit Design

- *IEEE/ACRC Workshop on Memristors and Resistive Memory Devices and Applications in Computer Architecture and Brain-Inspired Systems*, Technion - Israel Institute of Technology, Haifa, Israel, March 2012.

Memristors and Related Applications

- *The International Conference of the Israeli Semiconductor Industry (ChipEx 2011)*, Tel Aviv, Israel, May 2011.

Posters

1. E. Giacomin, T. Greenberg-Toledo, **S. Kvatinsky**, and P.-E. Gaillardon, "A Robust Digital RRAM-based Convolutional Block without Process Variation Dependencies," *Design Automation Conference*, June 2018.
2. N. Wainstein and **S. Kvatinsky**, "RF Memristor Modeling," *International Conference on Memristive Materials, Devices & Systems*, April 2017.
3. R. Ben-Hur and **S. Kvatinsky**, "Processing within a Memristive Memory," *Proceedings of the International Workshop on Emerging Memory Solutions, DATE Conference*, March 2016.

4. D. Soudry, D. Di Castro, A. Gal, A. Kolodny, and **S. Kvatinsky**, "Implementing Hebbian Learning Rules with Memristors," *Workshop on "Memristor-based Systems for Neuromorphic Applications,"* September 2013.
5. **S. Kvatinsky**, E. G. Friedman, A. Kolodny and U.C. Weiser, "Memristor-based Logic," *MemCo Workshop - Memristors for Computing*, November 2012.
6. **S. Kvatinsky**, E. G. Friedman, A. Kolodny and U.C. Weiser, "Memristor-based Circuits and Architectures," *2nd Technion Computer Engineering (TCE) Conference*, June 2012.
7. **S. Kvatinsky**, E. G. Friedman, A. Kolodny and U.C. Weiser, "Memristor-based Applications," *1st Technion Computer Engineering (TCE) Conference*, June 2011.