November 2024

CURRICULUM VITAE
Shahar Kvatinsky

Personal Details

Work Address: Viterbi Faculty of Electrical and Computer Engineering
Technion – Israel Institute of Technology
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http://asic2.group

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Academic Degrees

2014 *Ph.D. Electrical Engineering, Technion*
Dissertation Title: "Memristor-based Circuits and Architectures".
Direct track degree.
Advisors: Prof. Avinoam Kolodny, Prof. Eby Friedman, and Prof. Uri Weiser.

2010 *MBA Business Administration, Hebrew University, Jerusalem*
Graduated Magna Cum Laude, GPA: 94.8/100.
Specialized in business strategy and entrepreneurship, and finance and banking.

2009 *B.Sc. Computer Engineering and Applied Physics, Hebrew University, Jerusalem*
Graduated Magna Cum Laude, GPA: 96.6/100.
Specialized in microelectronics and optoelectronics.

Academic Appointments

7/2023 – now *Visiting Professor*
Electrical and Computer Engineering, University of Toronto

4/2024-now *Full Professor*
Electrical and Computer Engineering, Technion

11/2019-3/2024 *Associate Professor*
Electrical and Computer Engineering, Technion

7-8/2018 *Visiting Assistant Professor*
Electrical and Computer Engineering, University of Utah

10/2015-10/2019 *Assistant Professor*
Electrical Engineering, Technion
Viterbi fellow at the Technion Computer Engineering Center.

2014-2015 *Post Doctoral Researcher*
Computer Science, Stanford University

Professional Experience

2007-2009 *Circuit designer at Intel, Jerusalem.*

Research Interests

VLSI, computer architecture, digital circuits, analog circuits, memory design, hardware for machine learning, neuromorphic computing, cytomorphic computing, system-on-a-chip, FPGA, hardware-software interface, emerging non-volatile memory technologies, EDA, hardware security, superconductor logic.

Teaching

University of Toronto

2024	Computer Architecture (undergraduate level)	Lecturer

Technion

2019-2023	*Digital Systems and Computer Organization* (undergraduate level)	Lecturer (in charge)
2018	*Advanced Topics in Computer Engineering* (graduate level, new, with Mark Silberstein and Yoav Etsion)	Lecturer
2017-2023	*Seminar in VLSI Systems* (graduate level)	Lecturer
2016-2023	*Circuits and Architectures with Memristor* (undergraduate and graduate level, new)	Lecturer
2015-2018	*Logic Design and Introduction to Computers* (undergraduate level)	Lecturer (in charge)
2015-2016	*Advanced Topics in Computer Design* (graduate level, new)	Lecturer
2011-2014	*Computer Architecture* (undergraduate and graduate level)	Teaching assistant (in charge)
2011-2014	*Advanced VLSI Architectures* (undergraduate and graduate level)	Teaching assistant (in charge)
2009-2013	*Linear Electronics Circuits* (undergraduate level)	Teaching assistant
2009-2014	*SOPC (System on a Programmable Chip) lab* (undergraduate level)	Instructor
2010-2014	*B.Sc. projects, VLSI laboratory* (undergraduate level)	Supervisor

Received commendation as a lecturer (Spring 2018), won six times the Technion excellence award for teaching assistants (Spring 2010, Winter 2011, Spring 2011, Spring 2012, winter 2013, Spring 2014). Supervised the winning projects in the Yehoraz Kasher annual EE project contest in 2011, the Oz Mozes prize in 2012, and the Seiden Prize 2015.

The Hebrew University, Jerusalem.

2009	*Physics Lab for Engineers* (undergraduate level)	Instructor

Professional Service Activities

National Activities

2022	Israel Science Foundation scientific committee
2022-2023	Alon Fellowship committee
2021-2022	Committee on VLSI engineers in Israel

Technion Activities

2022-2023	New faculty mentorship program leader (with Prof. Tamar Segal-Peretz and Noa Nof-Steiner)
2021-2022	New faculty mentorship program leader (with Prof. Yoav Shechtman and Prof. Galit Yom-Tov)
2020-2023	Technion undergraduate entrepreneurship and innovation committee member
2019-2023	Technion Hiroshi Fujiwara cyber security research center scientific committee member

Departmental Activities

2020-2023	Entrepreneurship coordinator
2019-2023	Master studies acceptance committee
2019-2020	Undergraduate best project committee
2018-2023	Graduate studies committee
2016-now	Head of the Architecture and Circuits Research Center (ACRC)
2018-2023	Undergraduate students' consultant for the VLSI and circuits chain
2015-2019	Undergraduate students' consultant for 1st year students
2015-2018	Undergraduate students' consultant for the computer engineering track and the computers chain

Associate Editor

2018-2024	Array, Elsevier
2014-now	Microelectronics Journal, Elsevier

Guest Editor

IET Electronics Letters – Special issue on "Memristive Electronic Circuits, Neural Networks and Neuromorphic Computing" (co-editors Yichuang Sun, University of Hertfordshire, Georgios Sirakoulis, Democritus University of Thrace, Jingru Sun, Hunan University)

Frontiers in Neuroscience – Special issue on "Advances in Highly Efficient Neuromorphic Computing with Emerging Memory Devices" (co-editors Nan Du, TU Chemnitz, Wei Wang, Technion, and Yuriy Pershyn, University of South Carolina).

MDPI Applied Sciences - special issue on "Advances in Brain-Inspired Computing" (co-editors Elishai Ezra Tsur, the Open University of Israel and Ehud Ahissar, Weizmann Institute).

IEEE Nanotechnology Magazine – special issue on "Novel Applications Enabled by Memristors" (co-editor Marco Ottavi, University of Rome Tor Vergata).

IEEE Embedded Systems Letters – special issue on "Embedded Nano-Security" (co-editors Farhad Merchant and Rainer Leupers, RWTH Aachen University).

Program Committee Chair
GLSVLSI 2025.
VLSI-SoC 2020.

Topic Program Committee Chair
DATE 2020, 2021, 2022 (topic D15 – Emerging Design Technologies for Future Memories).

Tutorials and Workshops Chair
HPCA 2018.

Program Committee
IEEE ISACC 2025, VLSID 2025, E2A 2024, E2A 2023, ICONS 2023, ICONS 2022, DAC 2022, ICONS 2021, DAC 2021, VLSID 2021, NVMW 2021, DAC 2020, CIMW 2020, NVMW 2020, VLSID 2020, eMTDT 2019, MEMRISYS 2019, SPACE 2019, VLSI-SoC 2019, DATE 2019, APCCAS 2018, VLSI-SoC 2018, MDAC in HiPEAC 2017, 2018, DATE 2018, MemTCAD in HiPEAC 2015, 2016, ChipEx 2016.

PhD Committee
1. Elisheva Berkovich, Bar Ilan University, 2023.
2. Emmanuel Bender, Ariel University, 2022.
3. Ilan Oren, Technion 2022.
4. Or Levit, Technion, 2022.
5. Itamar Melamed, Technion, 2021.
6. Erez Zolkov, Technion, 2021.
7. Oren Kalinsky, Technion, 2020.
8. Itay Hubara, Technion, 2019.
9. Nimrod Ginzberg, Technion, 2019, 2022.
10. Ayal Eshkoli, Technion, 2018.
11. Gil Shomron, Technion, 2018.
12. Binyamin Frankel, Bar Ilan University, 2018.
13. Roman Kaplan, Technion, 2017.
14. Oron Port, Technion, 2017.
15. Robert Gitterman, Bar Ilan University, 2016.
16. Evripides Kyriakides, University of Nicosia, Cyprus, 2016.

MSc Committee
1. Igor De Paula, Technion, 2023.
2. Mohammad Hadish, Technion, 2023.
3. Avi Hazan, Open University, 2021.
4. Itamar Melamed, Technion, 2020.
5. Natan Vinshtok-Melnik, Bar Ilan University, 2020.
6. Hanna Abu Hanna, Technion, 2019.
7. Tsahi Noy, Bar Ilan University, 2019.
8. Daniel Vana, Tel Aviv University, 2019.
9. Iliah Konstantinovsky, Technion, 2019.
10. Roy Weiss, Technion, 2018.
11. Yuval Ben-Hur, Technion, 2018.
12. Amit Kazimirsky, Bar Ilan University, 2016.
13. Kfir Mizrahi, Technion, 2017.
14. Oren Nishri, Technion, 2017.

Workshop, Tutorials, and Training School Organizer

2024 *Nano Security: From Nano-Electronics to Secure Systems*
Workshop in DATE (Antwerp, Belgium)
Co-organizers: Ilia Polian (University of Stuttgart), Nan Du (IPHT Jena), and Ingrid Verbauwhede (KU Leuven)

2023 *Memristive Digital Processing-in-Memory*
Tutorial at ISCAS (Monterey, California, USA)

2023 *AI on Chip* (Tel Aviv, Israel)
Co-organizer: Raja Giryes (Tel Aviv University)

2023 *Nano Security: From Nano-Electronics to Secure Systems*
Workshop in DATE (Antwerp, Belgium)
Co-organizers: Ilia Polian (University of Stuttgart), Nan Du (IPHT Jena), and Ingrid Verbauwhede (KU Leuven)

2022 *Memristive Digital Processing-in-Memory*
Tutorial at ICECS (Glasgow, United Kingdom)

2019 *Real Processing-in-Memory with Memristive Memory Processing Unit*
Tutorial at SPACE (India)

2018 *Analog Mixed-Signal Circuit Design with Memristors*
Tutorial at ISCAS (Italy)

2017 *Mixed Signal Circuit Design with Memristors*
Tutorial at IEEE COMCAS (Tel Aviv, Israel)

2017 EU COST Action IC-1401
Training school at the Technion (Haifa, Israel)

2017 *Stephen and Sharon Seiden Frontiers in Engineering and Science Workshop: Beyond CMOS: From Devices to Systems*
Workshop (Haifa, Israel)
Co-organizers: Eby Friedman (Rochester) and Avinoam Kolodny (Technion)

2016 *In-Memory and In-Storage Computing with Emerging Technologies*
Workshop in PACT (Haifa, Israel)
Co-organizer: Leonid Yavits (Technion)

Special Session Organizer

2022 *Secured Neuromorphic Computing* ISVLSI
Co-organizer: Minhui Zou (Technion)

2019 *Synthetic Biology – when Biology and Electronics Meet* BioCAS
Co-organizers: Ramez Danial (Technion) and Yosi Shacham-Diamand (Tel Aviv University)

2017 *Memristor for Computing: Myth or Reality?* DATE
Co-organizers: Said Hamdioui (TU Delft) and Gert Cauwenberghs (UCSD)

2016 *Memristors for Computing* CNNA
Co-organizer: Dietmar Fey (FAU).

Scientific Advisory Board

- Chua Memristor Center (CMC) at TU Dresden, Germany.
- International Advisory Board of the 3rd International Conference "Emerging Materials, Technologies and Applications for Non-volatile Memory Devices"

- DFG-funded Priority Program "Nano Security: From Nano-Electronics to Secure Systems".
- Advanced Intelligent Systems (Editorial Advisory Board)

Journal/Conference Referee

1. 17th International Conference on Digital Signal Processing (DSP 2011).
2. 39th International Symposium on Computer Architecture (ISCA 2012).
3. Microelectronics Journal.
4. IEEE Transactions on Nanotechnology.
5. 7th International Symposium on Networks-on-Chip (NOCS 2013).
6. Reed-Muller Workshop (RM 2013).
7. IEEE International Symposium on Circuits and Systems (ISCAS) 2013.
8. Radioengineering.
9. PLOS ONE.
10. IEEE International Symposium on Circuits and Systems (ISCAS) 2014.
11. IEEE Transactions on Electron Devices.
12. Journal of Circuits, Systems, and Computers.
13. IEEE Transactions on Circuits and Systems I: Regular Papers.
14. IEEE Transactions on Circuits and Systems II: Express Briefs.
15. IEEE Transactions on Very Large Scale Integration (VLSI).
16. IEEE Transactions on Neural Networks and Learning Systems.
17. IEEE Journal on Emerging and Selected Topics in Circuits and Systems.
18. International Journal of Electronics and Communications.
19. IEEE Electron Device Letters.
20. Frontiers in Neuroscience.
21. The 48th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO 2015).
22. BIOCAS 2015.
23. IEEE International Symposium on Circuits and Systems (ISCAS) 2016.
24. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems.
25. IEEE Transactions on Emerging Topics in Computing.
26. ACM Journal on Emerging Technologies in Computing Systems.
27. IET Circuits, Devices, & Systems.
28. International Workshop on Cellular Nanoscale Networks and their Applications (CNNA) 2016.
29. Neural Computing and Applications (NCAA).
30. IEEE International Symposium on Circuits and Systems (ISCAS) 2017.
31. Electronics Letters.
32. High Performance Computer Architecture (HPCA) 2018.
33. IEEE International Symposium on Circuits and Systems (ISCAS) 2018.
34. Nature Nanotechnology.
35. Nature Electronics.
36. Nature Communications.
37. High Performance Computer Architecture (HPCA) 2019.
38. IEEE International Symposium on Circuits and Systems (ISCAS) 2019.
39. IEEE Computer Architecture Letters.
40. IEEE International Conference on Electronics Circuits and Systems (ICECS) 2019.
41. Advanced Intelligent Systems.
42. Physica Status Solidi A: Applications and Materials Science
43. IEEE International Symposium on Circuits and Systems (ISCAS) 2021.
44. IEEE Journal of the Electron Devices Society.
45. Advanced Science.

Grants Referee

1. Israel Science Foundation.
2. Deutsche Forschungsgemeinschaft (DFG).

Membership in Professional Societies

IEEE (senior member).
IEEE Israel Circuits and Systems chair.
IEEE Cellular Nanoscale Networks and Memristor Array Computing Technical Committee.

Military Service

1999-2004 *Officer in the IDF, rank: Lieutenant Colonel.*
Participated in several courses and training including sergeant course, officer course, and company commander course and served in several commanding positions including an artillery battery commander and artillery officer course commander.
Currently in the reserve forces.

Fellowships, Awards and Honors:

2023	HiPEAC 2023 Paper Award
2023	Uzi & Michal Halevy Award for Innovative Applied Engineering
2023	Best poster award at the International Meeting on Ferroelectricity 2023.
2022	Nominations for the best paper award and best student paper award, IEEE International Conference on Modern Circuits and Systems Technologies (MOCAST)
2021	Device Research Conference best student poster award
2021	Norman Seiden Prize for Academic Excellence
2021	**Elected as a member of the Israel Young Academy**
2021	Hershel Rich Technion Innovation Award
2020	Most cited paper in 5 years, *IEEE Transactions of Circuits and Systems II: Express Briefs*
2020	Paper selected among top 15 papers in the VLSI-SoC conference to appear in the VLSI-SoC book
2020	MDPI Electronics Young Investigator Award
2020	Jacobs Best Paper (Technion award for best paper by a graduate student in engineering)
2020	Selected as "one of the 20 promising Israelis of the next decade" by Yedioth Aharonot
2019	Paper selected among top 18 papers in the VLSI-SoC conference to appear in the VLSI-SoC book
2019	Best poster award in Neuromorphic Computing – A Nature Conference
2019	Alexander Goldberg Research Prize Fund (Technion)
2019	**Wolf Foundation Krill Prize for Excellence in Scientific Research**
2018	Commendation as a lecturer (top 12% at the Technion)
2018	KLA-Tencor Excellent Conference Paper Award
2017	**European Research Council starting grant**
2017	**Pazy Memorial Research Award for "the most outstanding and original BSF supported project in mathematical and computer sciences"**
2017	Hershel Rich Technion Innovation Award

2016	Paper selected among top 10 papers in the VLSI-SoC conference to appear in the VLSI-SoC book
2015	Supervised the Seiden Prize for Multidisciplinary Undergraduate Projects in Nano Electronics
2015-2018	Viterbi Fellowship in the Center for Computer Engineering at the Technion
2015	Best Paper of Computer Architecture Letters Award
2015	Supervised the 3rd place winning project in the Yehoraz Kasher Annual EE Project Contest
2015	**IEEE Guillemin-Cauer Best Paper Award**
2015	Viterbi Fellowship for Nurturing Future Faculty Members
2014	Hershel Rich Technion Innovation Award
2014	The Andrew and Erna Finci Viterbi Fellowship
2013, 2014	Vivian Konigsberg Award for Excellence in Teaching (twice)
2013	Sanford Kaplan Prize for Creative Management in High Tech in the 21st Century – 1st place
2013	Best lecturer award – ChipEx 2013
2012	Supervised the winning project in the Oz Mozes Project Contest
2012	Intel award for excellence in research
2011	Vivian Konigsberg Award for Excellence in Teaching (twice)
2011-2014	Hasso Plattner Institute Fellowship (four years)
2011	Irwin and Joan Jacobs Fellowship
2011	Supervised the winning project in the Yehoraz Kasher Annual EE Project Contest
2010, 2012	Sandor Szego Award for Excellence in Teaching (twice)
2010	Benin prize for graduate students
2010	The Marker MBA Case Study Competition finalist
2009	"Peter Brojde Center for Innovative Engineering and Computer Science" excellence final B.Sc. project prize
2007, 2008	Dean's reward for excellence, Hebrew University (twice)
2006-2009	Dean's honorary list, Hebrew University (all four years)

Students Supervised

Completed PhD theses

2024	Rotem Ben-Hur	*Enhancing Computer Performance with memristive Memory Processing Units: From General-Purpose Automation to DNA Sequencing Acceleration*
2024	Tzofnat Greenberg-Toledo	*Memristive Artificial Neural Network Accelerator with Online Training* Co-advisor: Daniel Soudry First employment with Nvidia
2023	Ben Perach	*Architecture for Bulk Bitwise Processing-in-Memory* First employment with Nvidia
2021	Nicolas Wainstein	*RF Front-End Circuits Based on Memristive Devices* Co-advisor: Eilam Yalon First employment with Intel

2021	Loai Danial	*Neuromorphic Data Converters using Memristors* First employment with Intel

Completed MSc theses

2023	Issa Salameh	*Superconductive Logic using Half Flux Quantum Pulses*
2023	Marcel Khalifa	*Acceleration of Bioinformatics Applications Using Memristive Processing-in-Memory Architecture*
2021	Mor Dahan	*Design of Ferroelectric FET Memories* First employment a PhD student at the Technion
2021	Adi Eliahu	*Programmable Processing-in-Memory Memristive Architectures* First employment with Apple
2018	Nimrod Wald	*Use of Memristor Based Logic Circuits for Beyond von Neumann Computer Architectures* First employment with Terrain EDA
2018	Ameer Haj Ali	*Performing Image Processing in Memristive Memory Arrays* First employment a PhD student at UC Berkeley
2018	Nishil Talati	*Logic Design for non-von Neumann Architectures using Memristors* First employment a PhD student at University of Michigan
2017	Misbah Ramadan	*Adaptive Programming for Multi-Level Cell ReRAM* Co-advisor: Ran Ginosar First employment with Apple
2015	Yifat Levy	*Logic with Memristive Akers Arrays* Co-advisors: Avinoam Kolodny and Eby Friedman First employment with Intel

PhD theses in progress

2020-2024	Lior Rodes	*Thermoelectic PUFs* Co-advisor: Eilam Yalon
2018-2024	Barak Hoffer	*Chip Design of Memristive Memory Processing Unit*
2021-2024	Orian Leitersdorf	*Advancing Computer Science with Memristive Processing-in-Memory*

MSc theses in progress

2022-2024	Sariel Hodisan	*Novel Analog Circuits Using Memristors and New Emerging Devices*
2023-2025	Rishona Daniels	*Reservoir Computing with Memristive Neural Networks*
2022-2025	Duna Wattad	*A Development of Mechanisms for Detection and Mitigation of Asymmetric Transistor Aging*
2023-2025	Ofri Levin	*Accelerating Graph Neural Networks with Memristors*

Post-docs

2021-2023	Minhui Zou	
2021-2022	Anindita Chakraborty	First employment Assistant Professor in Siksha 'O' Anusandhan University
2020-2021	Wei Wang	First employment Senior Researcher in Peng Cheng Laboratory, China
2019-2020	Kunal Korgaonkar	First employment Assistant Professor in BITS Pilani, India
2017-2018	John Reuben	First employment Associate Professor in Vellore Institute of Technology, India

Sponsored Long-Term Visitors

June 2023-October 2024	Tanay Patni *BITS Pilani, India*	Visiting scholar
January-June 2023	Arjun Tyagi *BITS Pilani, India*	Visiting scholar
October 2022--October 2024	Jiang Li *Nanjing University, China*	Visiting scholar
October 2022-March 2023	Henriette Padberg *RWTH Aachen, Germany*	Visiting scholar
September 2022-May 2023	Thomas Neuner *TU Munich, Germany*	Visiting scholar
July 2022-February 2023	Rishona Daniels *Mumbai University, India*	Visiting scholar
September-December 2021	Devangshu Datta *National Institute of Technology, Jamshedpur, India*	Visiting scholar
September-December 2021	Sumukh Pinge *BITS Pilani, India*	Visiting scholar
March-August 2021	Aatman Borda *BITS Pilani, India*	Visiting scholar
January-June 2020	Ruchi Dhamnani *International Institute of Information Technology, Naya Raipur, India*	Visiting scholar
January-June 2020	Parul Damahe *International Institute of Information Technology, Naya Raipur, India*	Visiting scholar
January-June 2020	Purvi Agrawal *International Institute of Information Technology, Naya Raipur, India*	Visiting scholar
June-August 2019	Rajaie Ismeeh *Bir Zeit University, Ramallah, Palestinian Territories*	Visiting scholar
May-July 2019	Anmol Jain *Indian Institute of Technology, Roorkee, India*	Visiting scholar
May-December 2019	Jeffrey Louis *BITS Pilani, India*	Visiting scholar
May – November 2019	Shivansh Dwivedi *Indian Institute of Technology, Indore, India*	Visiting scholar

May – November 2019	Kanishka Sharma *Indian Institute of Technology, Indore, India*	Visiting scholar
October 2018-May 2019	Varun Tandon	Visiting scholar
July-September 2018	Debjyoti Bhattacharjee *Nanyang Technological University, Singapore*	Visiting scholar
June 2018-May 2019	Kunal Korgaonkar *University of California, San Diego*	Visiting scholar
May-July 2018	Vasu Gupta *BITS Pilani, India*	Visiting scholar
May-July 2018	Sidharth Thomas *Indian Institute of Technology, Roorkee, India*	Visiting scholar
May-July 2018	Keshav Tiwari *Indian Institute of Technology, Roorkee, India*	Visiting scholar
December 2016-January 2017	Elias Cohen *Reed College, Oregon*	Visiting scholar
May-July 2016	Nishil Talati *BITS Pilani, India*	Visiting scholar

B.Sc. Projects

1. Dmitry Belousov and Slavik Liman, "Memristor-based Circuits" (*Winners of the Yehoraz Kasher EE Project Contest*).
2. Zahi Lahti and Elad Osherov, "Memristor Model."
3. Oren Lev and Emanuel Darji, "Analysis of Power Grids."
4. Keren Talisveyberg and Dmitry Fliter, "Memristor Verilog-A and MATLAB Modeling."
5. Ilan Shusterman and Michael Rozenblat, "Memristor-based Memory Analysis."
6. Leon Karbachevsky and Boaz Blankrot, "Memristor-based Analog Circuits."
7. Guy Satat and Nimrod Wald, "Memristor-based Full Adder," "Memristor-based Multithreading Processor" (*Winners of the Oz Mozes Project Contest*).
8. Boris Bashkansky and Lahav Madlinsky, "Memristor-based Memory Array Circuit and Layout Design."
9. Rotem Tabach and Dina Leshinsky, "Neuromorphic Systems."
10. Yiffah Fishler and Shir Lindenbaum, "Memristor Modeling."
11. Firas Shama and Louie Matar, "Memristor-based Multithreading Processor."
12. Keren Tendeter and Shiran Shuster, "Simulator for Memristor-based Memory."
13. Misbah Ramadan and Loai Danial, "Analysis of a Memristor-based Crossbar."
14. Hani Bezalel and Rotem Gabay, "Controller for Memristor-based Logic."
15. Benny Fellman and Gilad Tsoran, "Memristor-based Multithreading Processor."
16. Moab Arar and Muhammad Grefat, "Simulation Tools for Emerging Memory Technologies."
17. Israel Goldstein and Alex Dozortzev, "Memristor-based Crossbar for Neural Networks."
18. Misbah Ramadan, "Memristor Modeling."
19. Yoav Furman and Rula Naffaa, "Complementary MRL."
20. Avishay Drori and Elad Amrani, "Logic Design with Memristive Devices."
21. Eyal Rosenthal and Sergey Greshnikov, "Machine Learning with Memristors."
22. Itay Tsabari, "DNA Sequencing by Logic within Memory."
23. Adi Eliahu, "PulpFiction."
24. Barak Hoffer, "Testing of Memristive Memory Processing Unit."
25. Liora Huf, "Single Flux Logic Survey."

<u>Research Grants</u> (Total Funding 2015-2024: $6,150,000)

Competitive

2024-2026 *MAGNET consortium - NeMO - Israel Innovation Authority*
(958K NIS for 1.5 years, co-PI Nicolas Wainstein)

2024 *European Research Council Proof of Concept*
Real Database PIM
(Total funding 150K Euro for 1 year).

2023-2025 *KAMIN - Israel Innovation Authority* Project no. 81755
Transimpedance Amplifier with Automatic Gain Control
(880K NIS for 2 year)

2022 *European Research Council Proof of Concept* Grant no. 101069336
Real Processing in Phase Change Memory
(Total funding 150K Euro for 1 year).

2021-2024 *NSF-BSF*
Reliable and Zero-Power Timkeepers for Intermittently Powered Computing Devices via Stochastic Magnetic Tunnel Junctions
Co-PIs: Josiah Hester and Pedram Khalili (Northwestern University)
(Total funding $800K for 3 years, Technion's part $240K)

2022-2024 *Technion Human Health Institute*
Harnessing Synthetic Biology and Ultra-Low Power Electronics to Monitor Environmental Signals in the Gastrointestinal Tract
Co-PIs: Naama Geva-Zatorsky, Hossam Haick, Eilam Yalon, and Ramez Daniel
(Total funding $500K for 2 years, Kvatinsky's part $100K)

2021-2024 *NSF-BSF*
Reliable and Zero-Power Timekeepers for Intermittently Powered Computing Devices via Stochastic Magnetic Tunnel Junctions
Co-PIs: Josiah Hester and Pedram Khalili (Northwestern University)
(Total funding $800K for 3 years, Technion's part $240K)

2021-2022 *Peter Munk Research Institute*
Design and Characterization of Sneak Path Coating Based Physical Unclonable Function
Co-PI: Eilam Yalon (Technion)
(Total funding 100K NIS for 1 year)

2021-2024 *EU H2020-FETOPEN*
NEU-ChiP
Co-PI (Technion): Ramez Daniel

(Total funding 3.46M Euro for 3 years, Technion's part 400K Euro)

2020-2021 *Polak Fund for Applied Research*
Intelligent Analog-to-Digital Converter using Emerging Memory
($30K for 1 year)

2019-2021 *KAMIN - Israel Innovation Authority* Project no. 66769
Memristor-Based Reconfigurable RF Circuits
(887K NIS for 2 year)

2019-2020 *Technion Hiroshi Fujiwara cyber security research center and the Israel cyber bureau*
(140K NIS for 1 year)

2018-2021 *MAGNET consortium - GenPro - Israel Innovation Authority*
(835K NIS for 3 years)

2018-2020 *Technion Hiroshi Fujiwara cyber security research center and the Israel cyber bureau*
Co-PI: Avi Mendelson (Technion)
(300K NIS for 3 years)

2018-2019 *Julia and Joshua Ruch Exchange Program*
Co-PI: Zhiru Zhang (Cornell)
($7K for traveling)

2018-2022 ***European Research Council Starting Grant*** Grant no. 757259
Memristive In-Memory Processing Systems
(1.5M Euro for 5 years)

2017-2021 *Israel Science Foundation (ISF)* Grant no. 1514/17
Design of Computer Memories with Independent Computing Capabilities
(1M NIS for 4 years)

2017-2020 *Ministry of Science and Technology*
Integrated Genetics and Memristors breaking through the scaling limits of Moore's law
Co-PI: Ramez Daniel (Technion)
(1.555M NIS for 3 years)

2017-2019 *US–Israel Binational Science Foundation (BSF)* Grant no. 2016016
High-Performance Normally-Off Parallel Processing
Co-PI: Pierre-Emmanuel Gaillardon (University of Utah)
($150K for 3 years)

2017-2019 *NSF-BSF* Grant no. 2015709
Dynamically Configurable Memory Technology Based on Ferroelectric-Gated FET's (FeFET's)
Co-PIs: Moshe Eizenberg (Technion) and Ma Tso-Ping (Yale University)
($150K for 3 years)

2017-2018 *Russell Berrie Nanotechnology Institute Nevet*
Integrated Genetics and Nanoelectronics Breaking through the Scaling Limits of Moore's Law
Co-PI: Ramez Daniel (Technion)
($40K for 1 year)

2017 *Israel Science Foundation equipment grant for new faculty* Grant no. 1515/17
(758,517 NIS)

2016-2018 *KAMIN - Israel Innovation Authority* Project no. 57681
Analog to Digital Converters with Memristive Neural Network
(840K NIS for 2 years)

2016-2019 *MAGNET consortium - HiPER - Israel Innovation Authority*
(700K NIS for 3 years)

2015-2018 ICT COST action
Memristors – Devices, Models, Circuits, Systems and Applications (MemoCIS)
(travel grants)

Industrial

2019-2020	*Western Digital* RISC-V Infrastructure ($48K NIS for 1 year)
2018-2019	*Huawei* ($200K for 1 years)
2017	*Cisco University Research Program Fund* Vulnerability Analysis of Emerging Nonvolatile Memory Technologies Co-PI: Avi Mendelson (Technion) ($80K for 1 years)
2015-2017	*Intel Collaborative Research Institute – Computational Intelligence* Memory Intensive Architectures ($137.5K for 2 years)

PUBLICATIONS (8017 citations, h-index 36, i10-index 84, students are underlined)

Thesis

S. Kvatinsky, "Memristor-Based Circuits and Architectures," PhD dissertation, August 2014.

Books Edited

1. *VLSI-SoC: Design Trends*, IFIP Advances in Information and Communication Technology, A. Calimera, P.-E. Gaillardon, K. Korganokar, **S. Kvatinsky**, R. Reis, (Eds.), Springer, 2021**.**

Refereed Journal Papers:

1. **S. Kvatinsky**, E. G. Friedman, A. Kolodny, and U. C. Weiser, "TEAM - ThrEshold Adaptive Memristor Model," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 60, No. 1, pp. 211-221, January 2013. ***2015 IEEE Guillemin-Cauer Best Paper Award.***
2. **S. Kvatinsky**, E. G. Friedman, A. Kolodny, and U. C. Weiser, "The Desired Memristor for Circuit Designers," *IEEE Circuits and Systems Magazine*, Vol. 13, No. 2, pp. 17-22, second quarter 2013.
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66. O. Leitersdorf, R. Ronen, and **S. Kvatinsky**, "ConvPIM: Evaluating Digital Processing-in-Memory through Convolutional Neural Networks Acceleration," (in review).
67. S, Hodisan, S. Ricci, D. Ielmini, and **S. Kvatinsky**, "Self-Automatic Gain Controlled Transimpedance Amplifier Utilizing Volatile Memristor," (in review).
68. Z. Fu, Y. Tang, Z. Mu, X. Lou, C. Wang, Z. Zhu, Z. Yuan, L. Jiang, **S. Kvatinsky**, W. Yu, X. Wei, S. He, E. Liu, X. Kou, and Y. Yang, "Implementation of Ray-Tracing Algorithm on Spintronic Random Number Generator," (in review).
69. N. Gusarov, R. Mandal, I. Salameh, I. Holzman, **S. Kvatinsky**, and Y. Ivry, "Low-power Rapid Planar Superconducting Logic Devices," (in review).
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Book Chapters:

1. N. Wald, E. Amrany, A. Drory, and **S. Kvatinsky**, "Logic with Unipolar Memristors: Circuits and Design Methodology," *VLSI-SoC: System-on-Chip in the Nanoscale Era – Design, Verification and Reliability*, IFIP Advances in Information and Communication Technology, T. Hollstein, J. Raik, S. Kostin, A. Tšertov, I. O'Connor, R. Reis (Eds.), Springer, Vol. 508, Chapter 2, pp. 24-40, 2017.
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19. A. Vasilyev, N. Bhagdikar, S. Richardson, A. Pedram, **S. Kvatinsky**, and M. Horowitz, "Evaluating Programmable Architectures for Image and Vision Applications," *Proceedings of the Annual ACM/IEEE International Symposium on Microarchitecture*, pp. 1-13, October 2016.
20. H. Ha, A. Pedram, S. Richardson, **S. Kvatinsky**, and M. Horowitz, "Improving Energy Efficiency of DRAM by Exploiting Half Page Row Access," *Proceedings of the Annual ACM/IEEE International Symposium on Microarchitecture*, pp. 1-12, October 2016.
21. R. Ben-Hur and **S. Kvatinsky**, "Memristive Memory Processing Unit (MPU) Controller for In-Memory Processing", *Proceedings of the IEEE International Conference on Science of Electrical Engineering*, pp. 1-5, November 2016.
22. N. Wald and **S. Kvatinsky**, "Design Methodology for Stateful Memristive Logic Gates," *Proceedings of the IEEE International Conference on Science of Electrical Engineering*, pp. 1-5, November 2016.
23. S. Hamdioui, **S. Kvatinsky**, G. Cauwenberghs, L. Xie, K. Bertels, N. Wald, S. Joshi, H. M. Elsayed, and H. Corporaal, "Memristor for Computing: Myth or Reality?" *Proceedings of the Design, Automation and Test in Europe*, pp. 722-731, March 2017.
24. **S. Kvatinsky**, R. Ben-Hur, N. Talati, and N. Wald, "mMPU: Memristive Memory Processing Unit," *International Conference on Memristive Materials, Devices & Systems*, April 2017.
25. L. Azriel and **S. Kvatinsky**, "Towards a Memristive Hardware Secure Hash Function (MemHash)", *Proceedings of the IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, pp. 51-55, May 2017.
26. N. Talati, Z. Wang, and **S. Kvatinsky,** "Rate-Compatible and High-Throughput Architecture Designs for Encoding LDPC Codes," *Proceeding of the IEEE International Symposium on Circuits and Systems*, pp. 1-4, May 2017.
27. N. Wainstein and **S. Kvatinsky**, "An RF Memristor Model and Memristive Single-Pole Double Throw Switches," *Proceeding of the IEEE International Symposium on Circuits and Systems*, pp. 1-4, May 2017.

28. J. Reuben, R. Ben Hur, N. Wald, N. Talati, A. Haj Ali, P.-E. Gaillardon, and **S. Kvatinsky**, "Memristive Logic: A Framework for Evaluation and Comparison," *Proceedings of the IEEE International Symposium on Power and Timing Modeling, Optimization and Simulation*, pp. 1-8, September 2017.
29. H. Abo Hanna, L. Danial, **S. Kvatinsky,** and R. Daniel, "Modeling Biochemical Reactions and Gene Networks with Memristors," *Proceeding of the IEEE Symposium on Biological Circuits and Systems*, pp. 1-4, October 2017.
30. R. Ben Hur, N. Wald, N. Talati, and **S. Kvatinsky**, "SIMPLE MAGIC: Synthesis and Mapping of Boolean Functions for Memristor Aided Logic (MAGIC)," *Proceeding of the IEEE International Conference on Computer Aided Design*, pp. 225-232, November 2017. ***KLA-Tencor Excellent Conference Paper Award.***
31. N. Talati, A. Haj Ali, R. Ben Hur, N. Wald, R. Ronen, P.-E. Gaillardon, and **S. Kvatinsky**, "Practical Challenges in Delivering the Promises of Real Processing-in-Memory Machines," *Proceedings of the Design Automation and Test in Europe*, pp. 1628-1633, March 2018.
32. A. Haj Ali, R. Ben-Hur, N. Wald, and **S. Kvatinsky**, "Efficient Algorithms for In-Memory Fixed Point Multiplication Using MAGIC," *Proceeding of the IEEE International Symposium on Circuits and Systems*, pp. 1-5, May 2018.
33. G. C. Adam, R. Badulescu, S. Iordanescu, N. Wainstein, and **S. Kvatinsky**, "A TiO_2 – Based Radio Frequency Resistive Switch," *Proceedings of the International Conference on Electron, Ion, and Photon Beam Technology and Nanofabrication*, June 2018.
34. L. Danial and **S. Kvatinsky**, "Real-Time Trainable Data Converters for General Purpose Applications," *Proceeding of the IEEE/ACM International Symposium on Nanoscale Architectures*, July 2018.
35. H. Abo Hanna, L. Danial, **S. Kvatinsky,** and R. Daniel, "Memristors as Artificial Biochemical Reactions in Cytomorphic Systems," *Proceedings of the IEEE International Conference on Science of Electrical Engineering*, December 2018.
36. B. Perach and **S. Kvatinsky**, "STT-ANGIE: Asynchronous True Random GEnerator Using STT-MTJ," *Proceedings of the Design, Automation and Test in Europe*, pp. 264-267, March 2019.
37. L. Danial, S. Thomas, and **S. Kvatinsky**, "Delta-Sigma Modulation Neurons for High-Precision Training of Memristive Synapses in Deep Neural Networks," *Proceedings of the International Symposium on Circuits and Systems*, pp. 1-5, May 2019.
38. N. Wainstein, T. Tsabari, Y. Goldin, E. Yalon, and **S. Kvatinsky**, "A Dual-Band CMOS Low-Noise Amplifier using Memristor-Based Tunable Inductors," *Proceedings of the IEEE Computer Society Annual Symposium on VLSI*, pp. 290-295, July 2019.
39. M. Ottavi, V. Gupta, S. Khandelwal**, S. Kvatinsky**, J. Mathew, E. Martinelli, and A. Jabir, "The Missing Applications Found: Robust Design Techniques and Novel Uses of Memristors," *Proceedings of IEEE International Symposium on On-Line Testing and Robust System Design*, pp. 159-164, July 2019.
40. **S. Kvatinsky**, "Real Processing-in-Memory with Memristive Memory Processing Unit (mMPU)," *Proceeding of the IEEE International Conference on Application-Specific Systems, Architectures and Processors*, July 2019.
41. J. Vieira, E. Giacomin, Y. Qureshi, M. Zapater, X. Tang, **S. Kvatinsky**, D. Atienza, and P.-E. Gaillardon, "A Product Engine for Energy Efficient Execution of Binary Neural Networks Using Resistive Memories," *Proceedings of the IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, October 2019 (in press). ***Selected for post-conference book (top 18 papers).***
42. L. Danial, K. Sharma, S. Dwivedi, and **S. Kvatinsky**, "Logarithmic Neural Network Data Converters using Memristors for Biomedical Applications," *Proceeding of the IEEE Symposium on Biological Circuits and Systems*, pp. 1-4, October 2019.
43. J. Louis, B. Hoffer, and **S. Kvatinsky**, "Performing Memristor Aided Logic (MAGIC) using STT-MRAM," *Proceedings of the IEEE International Conference on Electronics Circuits and Systems*, November 2019 (in press).

44. L. Danial, V. Gupta, E. Pikhay, Y. Roizin, and **S. Kvatinsky**, "Modeling a Floating-Gate Memristive Device for Computer Aided Design of Neuromorphic Integrated Circuits," *Proceedings of the Design, Automation and Testing in Europe*, March 2020 (in press).
45. N. Wainstein, G. Ankonina, **S. Kvatinsky**, and E. Yalon, "Nanosecond Probing of Phase Transition Properties in Chalcogenides using Embedded Heater-Thermometer," *Proceedings of the Materials Research Society Spring Meeting*, April 2020.
46. L. Danial and **S. Kvatinsky**, " Breaking the Conversion Wall in Mixed-Signal Systems Using Neuromorphic Data Converters," *Proceedings of the European Conference on Circuit Theory and Design*, pp. 1-4, September 2020.
47. L. Danial, K. Sharma, and **S. Kvatinsky**, "A Pipelined Memristive Neural Network Analog-to-Digital Converter," *Proceeding of the IEEE International Symposium on Circuits and Systems*, pp. 1-5, October 2020.
48. V. Gupta, D. Pellegrini, S. Khandelwal, A. Jabir, **S. Kvatinsky**, E. Martinelli, C. Di Natale, and M. Ottavi, "Sensing with Memristive Complementary Resistive Switch: Modelling and Simulations," *Proceedings of the IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems*, October 2020 (in press).
49. A. Eliahu, R. Ben Hur, R. Ronen, and **S. Kvatinsky**, "abstractPIM: Bridging the Gap Between Processing-in-Memory Technology and Instruction Set Architecture," *Proceedings of the IFIP/IEEE VLSI-SoC*, pp. 28-33, October 2020.
50. N. Peled, R. Ben-Hur, R. Ronen, and **S. Kvatinsky**, "X-MAGIC: Enhancing PIM with Input Overwriting Capabilities," *Proceedings of the IFIP/IEEE VLSI-SoC*, pp. 64-69, October 2020.
51. D. Bhattacharjee, A. Chattopadhyay, S. Dutta, R. Ronen, and **S. Kvatinsky**, "CONTRA: Area-Constrained Technology Mapping Framework for Memristive Memory Processing Unit," *Proceeding of the IEEE International Conference on Computer Aided Design*, pp. 1-9, November 2020.
52. **S. Kvatinsky**, "Making Real Memristive Processing-in-Memory Faster and Reliable," *Proceedings of the International Cellular Nanoscale Networks and their Applications*, pp. 1-3, October 2021.
53. M. Khalifa, R. Ben-Hur, R. Ronen, O. Leitersdorf, L. Yavits, and **S. Kvatinsky**, "FiltPIM: Filter in Memory for DNA Sequencing," *Proceedings of the IEEE International Conference on Electronics Circuits and Systems*, pp. 1-6, November 2021.
54. O. Leitersdorf, R. Ronen, and **S. Kvatinsky**, "Making Memristive Processing-in-Memory Reliable," *Proceedings of the IEEE International Conference on Electronics Circuits and Systems*, pp. 1-6, November 2021.
55. O. Leitersdorf, B. Perach, R. Ronen, and **S. Kvatinsky**, "Efficient Error-Correcting-Code Mechanism for High-Throughput Memristive Processing-in-Memory," *Proceedings of the Design Automation Conference*, December 2021.
56. O. Leitersdorf, R. Ronen, and **S. Kvatinsky**, "MatPIM: Accelerating Matrix Operations with Memristive Stateful," *Proceedings of the International Symposium on Circuits and Systems*, May 2022.
57. B. Oved, O. Leitersdorf, R. Ronen, and **S. Kvatinsky**, "HashPIM: High-Throughput SHA-3 via Memristive Digital Processing-in-Memory," *Proceedings of the IEEE International Conference on Modern Circuits and Systems Technologies*, June 2022.
58. M. Zou, J. Zhou, X. Cui, W. Wang, C. Wang, and **S. Kvatinsky**, "Security Enhancement for Memristor Computing System through Secure Weight Mapping," *Proceeding of the IEEE Computer Society Annual Symposium on VLSI*, July 2022.
59. B. Hoffer and S. Kvatinsky, "Performing Stateful Logic using Spin-Orbit Torque (SOT) MRAM," *Proceedings of the IEEE International Conference on Nanotechnology*, July 2022.
60. A. Gero, M. A. Hadish, and **S. Kvatinsky**, " Undergraduate Students' Attitudes Toward an Engineering Course that Integrates Several Levels of Abstraction," *Proceedings of the International Conference on Interactive Collaborative Learning and 51st International Conference on Engineering Pedagogy*, pp. 491-497, September 2022.

61. B. Perach, R. Ronen, and **S. Kvatinsky**, "On Consistency for Bulk-Bitwise Processing-in-Memory," *Proceedings of IEEE/ACM International Symposium on High-Performance Computer Architecture*, pp. 705-717, February 2023. ***HiPEAC 2023 Paper Award***
62. B. Perach, R. Ronen, and **S. Kvatinsky**, "Accelerating Relational Database Analytical Processing with Bulk-Bitwise Processing-in-Memory," *Proceedings of the IEEE Interregional NEWCAS Conference*, June 2023 (in press).
63. A. Gero, M. A. Hadish, and **S. Kvatinsky**, "Abstract Thinking of Beginning Electrical Engineering and Computer Science Students," *Proceedings of the International Conference on Interactive Collaborative Learning and 52nd International Conference on Engineering Pedagogy*, September 2023 (in press).
64. B. Perach, R. Ronen, and **S. Kvatinsky**, "Enabling Relational Database Analytical Processing in Bulk-Bitwise Processing-In-Memory," *Proceedings of the IEEE International System-on-Chip Conference*, September 2023 (in press).
65. N. Aflalo, E. Yalon, and **S. Kvatinsky**, "Bitwise Logic using Phase Change Memory Devices Based on the Pinatubo Architecture," *Proceedings of the International Conference on VLSI Design*, January 2024.
66. J. Li, Y. Cui, C. Wang, W. Liu, and **S. Kvatinsky**, "A Concealable RRAM Physically Unclonable Function Compatible with In-Memory Computing," *Proceedings of the Design, Automation and Testing in Europe*, March 2024.
67. A. Tyagi and **S. Kvatinsky**, "Assessing the Performance of Stateful Logic in 1-Selector 1-RRAM Crossbar Arrays," *Proceedings of IEEE International Symposium on Circuits and Systems*, pp. 1-5, May 2024.
68. N. Wainstein, A. Orren, R.-G. Harwood, E. Yalon, and **S. Kvatinsky**, "Asymmetric and Symmetric Single-Pole Double-Throw using Indirectly Heated Phase-Change Switches," *Proceedings of the International Conference on Microwaves, Communications, Antennas, Biomedical Engineering and Electronic Systems*, July 2024.
69. T. Patni, R. Daniels, and **S. Kvatinsky**, "Compact Behavioral Model for Volatile Memristors," *Proceedings of the IEEE International Conference on Flexible Electronics Technology*, September 2024.
70. D. Wattad, **S. Kvatinsky**, and F. Gabbay, "On-Die Telemetry Circuitry for Measuring Clock Tree Timing Deterioration Due to Asymmetric Transistor Aging," *Proceedings of the International Conference on Microelectronic Devices and Technologies*, September 2024.
71. O. Leitersdorf, R. Ronen, and **S. Kvatinsky**, "PyPIM: Integrating Digital Processing-in-Memory from Microarchitectural Design to Python Tensors," *Proceedings of the Annual ACM/IEEE International Symposium on Microarchitecture*, November 2024 (in press).
72. T. Neuner and **S. Kvatinsky**, "Realization of Memristor Ratioed Logic with HfO2-Based Resistive RAM," *Proceedings of the IEEE International Conference on Electronics Circuits and Systems*, November 2024.

Submitted Refereed Conference Papers:

73. R. Ben-Hur, R. Ronen, O. Leitersdorf, L. Goldshmidt, I. Magram, L. Kaplum, L. Yavits, and **S. Kvatinsky**, "DART-PIM: DNA read mApping acceleRaTor Using Processing-In-Memory," (in review).
74. B. Hoffer and **S. Kvatinsky**, "Stateful Logic In-Memory Using Gain-Cell eDRAM," (in review).

Magazines:

1. R. Daniel and **S. Kvatinsky**, "Combining Biology and Electronics Using Emerging Memristive Technologies," *Tower Jazz Technical Journal*, Vol. 8, pp. 30-38, June 2017.
2. **S. Kvatinsky**, "Computers that Look Like the Brain," *Frontiers for Young Minds*, Vol. 8, December 2020.

Technical Reports:

1. **S. Kvatinsky**, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Memristor-based IMPLY Logic Design Flow," *CCIT Technical Report #795*, August 2011.
2. **S. Kvatinsky**, K. Talisveyberg, D. Fliter, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Verilog-A for Memristor Models," *CCIT Technical Report #801*, December 2011.
3. **S. Kvatinsky**, E. G. Friedman, A. Kolodny, and U. C. Weiser, "TEAM - ThrEshold Adaptive Memristor Model," *CCIT Technical Report #80*4, January 2012.
4. D. Soudry, D. Di Castro, A. Gal, A. Kolodny, and **S. Kvatinsky**, "Hebbian Learning Rules with Memristors," *CCIT Technical Report #*840, September 2013.
5. **S. Kvatinsky**, M. Ramadan, E. G. Friedman, and A. Kolodny, "VTEAM - A General Model for Voltage Controlled Memristors," *CCIT Technical Report #*856, April 2014.
6. X. Yang, J. Pu, B. B. Rister, N. Bhagdikar, J. Ragan-Kelley, S. Richardson, **S. Kvatinsky**, A. Pedram, and M. Horowitz, "A Systematic Approach to Blocking Convolutional Neural Networks," *ArXiv:1606.04209,* June 2016.
7. R. Ben Hur, N. Wald, N. Talati, and **S. Kvatinsky**, " Latency Optimized Mapping of Logic Functions for Memristor Aided Logic (MAGIC)," *CCIT Technical Report #908*, December 2016.
8. K. Korgaonkar, R. Ronen, A. Chattopadhyay, and **S. Kvatinsky**, "Bitlet Model: Defining a Litmus Test for the Bitwise Processing-in-Memory Paradigm," *ArXiv:1910.10234*, October 2019.
9. T. Greenberg-Toledo, B. Perach, D. Soudry, and **S. Kvatinsky**, "MTJ-Based Hardware Synapse Design for Ternary Deep Neural Networks," *ArXiv:1912.12636*, December 2019.

Patents Granted:

1. S. Kvatinsky, Y. Levy, and A. Kolodny, "Memristive Akers Logic Array," US patent no. 9548741.
2. A. Kolodny, S. Kvatinsky, R. Patel, and E. G. Friedman, "Multistate Register Having a Flip Flop and Multiple Memristive Devices," US patent no. 9679650.
3. S. Kvatinsky, D. Belousov, S. Liman, N. Wald, and G. Satat, "A Pure Memristive Logic Gate," US patent no. 9685954.
4. D. Soudry, S. Kvatinsky, A. Gal, D. Di Castro, and A. Kolodny, "Implementating multiplication in adaptive circuits using memristive devices," US patent no. 9754203.
5. S. Kvatinsky, D. Belousov, S. Liman, N. Wald, and G. Satat, "Pure Memristive Logic Gate," US patent no. 10284203.
6. M. Ramadan, S. Kvatinsky, and R. Ginosar, "Adaptive Programming for Memories with Multi-Level Cells," US patent no. 103667526.
7. S. Kvatinsky, A. Kolodny, and U. C. Weiser, "Memristor-Based Multithreading," Israel patent no. 225988.
8. S. Kvatinsky, A. Kolodny, and U. C. Weiser, "Memristor-Based Multithreading," US patent application no. 10521237.
9. L. Azriel and S. Kvatinsky, "Memristive Security Hash Function," US patent no. 10708041.
10. A. Drori, E. Amrani, and S. Kvatinsky, " Logic Design with Unipolar Memristors," US patent no. 10516398.
11. A. Drori, E. Amrani, and S. Kvatinsky, "Logic Design with Unipolar Memristors," US patent no. 10855288.
12. A. Morad, L. Yavits, S. Kvatinsky, and R. Ginosar, "Hybrid Processor," US patent no. 10996959.
13. L. Danial and S. Kvatinsky, "Reconfigurable DAC Implemented by Memristor Based Neural Network," US patent no. 11611352.
14. L. Danial and S. Kvatinsky, "Analog-to-Digital Converter Using a Pipelined Memristive Neural Network," US patent no. 2021/0175893 A1.

15. T. Greenberg-Toledo, D. Soudry, and S. Kvatinsky, "MTJ-Based Hardware Synapse Implementation for Ternary and Binary Deep Neural Networks," US patent no. 2021/0174182.
16. L. Danial and S. Kvatinsky, "Delta-Sigma Modulation Neurons for High Precision Training of Memristive Synapses in Deep Neural Networks," US patent no. 2022/0058492 A1.
17. L. Danial and S. Kvatinsky, "Analog to Digital Converter using Memristors in a Neural Network," US patent no. 11720785.

Patents Filed:

18. B. Perach and S. Kvatinsky, "Asynchronous True Random Number Generator using STT-MTJ." US patent application no. 62/774,258.
19. P.-E. Gaillardon, E. Giacomin, and S. Kvatinsky, "A Robust Digital RRAM-based Convolutional Block for Low-Power Image Processing and Learning Applications," US patent application no. 62/734,023.
20. B. Hoffer and S. Kvatinsky, "Memristor Aided Logic (MAGIC) using Valence Change Memory (VCM)," US patent application no. 63/006,131.
21. S. Kvatinsky, B. Hoffer, E. Yalon, and N. Wainstein, "Logic Gates and Stateful Logic using Phase Change Memory," US patent application no. 63/006,114.
22. S. Kvatinsky, N. Wainstein, and E. Yalon, "Apparatus and Method for Ultra-Fast Crystallization in Phase-Change RF Switches," US patent application no. 20240313766.
23. S. Kvatinsky and S. Hodisan, "Transimpedance Amplifier with Automatic Gain Control Based on Memristors for Optical Signal Acquisition," US patent application no. 63/462,539.

Selected Talks (Plenary, Keynote, and Invited)

Real Digital Processing-in-Memory with the Memristive Memory Processing Unit

- The 5th International Conference on Memristive Materials, Devices, and Systems (MEMRISYS 2022), Cambridge, MA, USA, November 2022 (invited).

On-Device Machine Learning with Memristors in the Neuromorphic Era

- FENS symposium, Vienna, Austria, June 2024 (invited).
- CNRS AISSAI Workshop of Energetics of Computation in Artificial and Natural Networks, Paris, France, December 2022 (invited).
- Workshop on Neuromorphic Computing (NEUROCOM), HiPEAC conference, Budapest, Hungary, June 2022 (invited talk).
- SIRC "Designing Better Hardware with Artificial Intelligence," Samsung, Tel Aviv, Israel, December 2021 (keynote).

Making Real Memristive Processing-in-Memory Faster and Reliable

- International Conference on Emerging Electronics & Automation (E2A), NIT Silchar, India, December 2021 (keynote, virtual talk).
- The 7th Memristor and Memristive Symposium, Catania, Italy, October 2021 (invited talk).

Memristive Processing-in-Memory for Artificial Intelligence

- Faculty Development Program on Neuronal Dynamics and Neuromorphic Computing, Indian Institute of Technology, Patna, India (distinguished speaker, virtual talk), December 2021.
- Faculty Development Program on Neuronal Dynamics and Neuromorphic Computing, Indian Institute of Technology, Patna, India (distinguished speaker, virtual talk), October 2020.

Real Processing-in-Memory using Memristive Memory Processing Unit

- Faculty Development Program on Emerging Topics in Computing: Quantum, Microfluidic and Memristors, JIS University, Kolkata, India, August 2021 (invited talk, online).
- TEQIP-III Online Workshop on VLSI Based System Design, Indian Institute of Information Technology, Guwahati, India, March 2021 (invited, online).
- Huawei Compute and Storage Technology Conference 2020 (virtual), December 2020 (invited).
- Inaugural Chua Memristor Institute Conference (ICMIC), Wuhan, China, November 2019 (invited).
- International Conference on Memristive Materials, Devices and Systems, Dresden, Germany, July 2019 (keynote).
- IEEE International Symposium on Online Testing and Robust System Design, Rhodes, Greece, July 2019 (invited).
- IEEE International Conference on the Science of Electrical Engineering, Eilat, Israel, December 2018 (invited).
- In-Memory Computing: Emerging Devices, Architectures, and Applications, Politecnico di Torino, Italy, September 2018 (invited).
- 18th International Forum on MPSoC for Software Defined Hardware, Snowbird, UT, USA, August 2018 (plenary talk).
- International Conference on Neuromorphic Systems, Knoxville, Tennessee, USA, July 2018 (invited).
- The 8th Workshop on Systems for Multi-core and Heterogeneous Architectures, Porto, Portugal, April 2018 (keynote).
- Emertech 2018, Singapore, April 2018 (invited).

A Taxonomy and Evaluation Framework to Memristive Logic

- MemoCIS workshop, Dresden, Germany, September 2018 (plenary talk).

Logic Synthesis and Automation for Memristive Memory Processing Unit

- EPFL Workshop on Logic Synthesis and Emerging Technologies, Lausanne, Switzerland, September 2017 (invited).

Memristors for Learning

- IEEE International Conference on Science of Electrical Engineering, November 2016 (invited).

Computation with Memristors

- MemoCIS workshop, Palma de Mallorca, Spain, September 2016 (invited).

Introduction to Memristors

- ChipEx 2016, Tel Aviv, May 2016 (invited).

Avoiding the Dark Ages with Memristors

- MemoCIS Workshop: “Memristors: at the Crossroad of Devices and Applications”, Milan, March 2016 (keynote).

Emerging Memory Technologies: Challenges and Opportunities

- DesignEx 2015, Tel Aviv, November 2015 (invited).

Additional Selected Talks

The Return of Hardware: How Does Artificial Intelligence Changes the Computer Structure and the Education of Engineers?

- Talpiot College, Tel Aviv, Israel, February 2023 (virtual, colloquium).
- Out of the Box Conference, Achva College, Israel, March 2023 (plenary).

The Return of Hardware: How Does Artificial Intelligence Change the Computer Structure?

- Living in Science Fiction, Academix, Jerusalem, Israel, February 2023.

Memristive Neuromorphic Computing

- Umbrella Symposium, Aachen University, Aachen, Germany, May 2022 (invited).

Making Real Memristive Processing-in-Memory Faster and Reliable

- NextSilicon, September 2024 (virtual).
- University of Toronto, Toronto, Canada, March 2023 (invited seminar).
- McGill University, Montreal, Canada, February 2023 (invited seminar).
- Northwestern University, Evanston, Illinois, USA, November 2022 (invited seminar).
- IEEE Circuits and Systems Society Seasonal School on Intelligence in Chips: Integrated Sensors and Memristive Computing, November 2022 (virtual).
- Cadence, Israel, September 2022 (virtual).
- Nanjing University of Aeronautics and Astronautics, China, August 2022 (virtual).
- Aachen University, Aachen, Germany, May 2022 (invited seminar).
- Tel Aviv University, Tel Aviv, Israel, April 2022 (Electrical Engineering Department Colloquium).
- Hebrew University, Jerusalem, Israel, March 2022 (Applied Physics Department Colloquium).
- Marvel, Israel, March 2022 (virtual).
- Huawei Compute Technology Workshop, November 2021 (virtual, invited talk).

On-Device Machine Learning with Memristors in the Neuromorphic Era

- Israel Innovation Authority Workshop on Accelerators for AI, April 2021 (virtual, invited talk).
- Apple's Virtual Workshop on On-Device Machine Learning, April 2021 (virtual, invited talk).

Memristors in the Neuromorphic Era

- Weizmann Institute, Rehovot, Israel, February 2021 (virtual, invited seminar).

Real Processing-in-Memory using Memristive Memory Processing Unit

- George Washington University, Washington DC, USA, March 2024 (invited seminar).
- York University, Toronto, Canada, September 2023 (invited seminar).
- Pliops, Tel Aviv, Israel, July 2021.
- RWTH Aachen University, Germany, December 2020 (virtual, invited seminar).
- Universita' della Tuscia, Viterbo, Italy, March 2018.
- University of Rome Tor Vergata, Italy, March 2018.

Intelligent Trainable Data Converters

- SRC/SIA/DoE Workshop on New Trajectories for Analog Electronics, IBM Almaden, San Jose, CA, December 2019 (invited talk and panel).

Processing-in-Memory with Memristors

- Indian Institute of Technology, Delhi, India, December 2019 (seminar).

Memristors for Artificial Intelligence

- Bar Ilan University, Ramat Gan, Israel, April 2019 (department colloquium).
- Samsung, Ramat Gan, Israel, April 2019.

Designing Extremely Efficient Computers with Memristors

- Refael, Israel, September 2020.
- University of California, Irvine, CA, August 2018.
- University of Utah, Salt Lake City, Utah, July 2018.

Memristors: The Future of Non-Volatile Memory or Perhaps Even More?

- Nova, Rehovot, Israel, October 2021.
- Ramon Chips, Israel, August 2020 (virtual).
- Motorola Solutions, Airport City, Israel, September 2019.
- Intel, Jerusalem, Israel, January 2019.
- Applied Physics, School of Computer Engineering and Science, Hebrew University, Jerusalem, May 2018 (department colloquium).
- Department of Material Engineering and Science, Technion – Israel Institute of Technology, May 2018 (department colloquium).

Real Processing-in-Memory using Memristive Memory Processing Unit

- Universita' della Tuscia, Viterbo, Italy, March 2018.
- University of Rome Tor Vergata, Italy, March 2018.

Artificial Intelligence: Can a Computer Outsmart Humans?

- Italy-Technion Society event, Rome, Italy, March 2018 (invited).

A Taxonomy and Evaluation Framework to Memristive Logic

- MDAC HiPEAC, Manchester, United Kingdom, January 2018.

Memory Intensive Architectures

- Intel, Hillsborough, OR, USA, June 2017.

mMPU: Memristor Memory Processing Unit

- 2017 Stephen and Sharon Seiden Frontiers in Engineering and Science Workshop: Beyond CMOS: From Devices to Systems, Technion, Haifa, Israel, June 2017.
- Intel Collaborative Research Institute - Computational Intelligence Retreat, Haifa, Israel May 2017.

Computation with Memristors

- Intel, Haifa, Israel, December 2016.

Designing Extremely Energy Efficient Computers with Memristors

- 3rd Green Photonics Symposium, Technion, Haifa, Israel, March 2016.
- UT Dresden, Dresden, Germany, February 2016.
- Qualcomm, Haifa, Israel, January 2016.
- Mellanox, Yokneham, Israel, December 2015.
- Marvell, Petach Tikva, Israel, November 2015.
- Qualcomm, San Diego, July 2015.
- ARM, San Jose, CA, June 2015.
- UCLA, Los Angeles, CA, June 2015.
- UC Santa Barbara, Santa Barbara, CA, June 2015.
- Nvidia Research, Santa Clara, CA, May 2015.

- Intel Labs, Hillsborough, OR, May 2015.

Designing Extremely Energy Efficient Computers
- UT Austin, Austin, TX, March 2015.
- Technion – Israel Institute of Technology, Haifa, Israel, January 2015.
- Hebrew University of Jerusalem, Jerusalem, Israel, January 2015.
- Ben Gurion University of the Negev, Beer Sheva, Israel, January 2015.

Memory Intensive Computing
- Tel Aviv University, Tel Aviv, July 2014.
- *DATE 2014*, Dresden, Germany, March 2014.
- *HiPEAC 2014*, Vienna, Austria, January 2014.

Building the Computers of the Future – a Talk about Resistors, Memories, and More
- *Jacobs Showcase Lecture Series: Much is New Under the Sun*, Technion - Israel Institute of Technology, Haifa, Israel, November 2013.

Memristors – Not Only Memory
- Princeton University, NJ, September 2013.
- Columbia University, NY, September 2013.
- Stanford University, Stanford, CA, September 2013.
- UC Berkeley, Berkeley, CA, September 2013.
- HP Labs, Palo Alto, CA, September 2013.
- UC San Diego, La Jolle, CA, September 2013.
- UC Santa Barbara, Santa Barbara, CA, October 2013.
- *The International Conference of the Israeli Semiconductor Industry (ChipEx 2013)*, Tel Aviv, Israel, May 2013. **Best lecture award**.

The Desired Memristor for Circuit Designers
- *Nature Conference on "Frontiers in Electronic Materials: Correlation Effects and Memristive Phenomena*," Aachen, Germany, June 2012.

Memristor-based Logic Circuit Design
- *IEEE/ACRC Workshop on Memristors and Resistive Memory Devices and Applications in Computer Architecture and Brain-Inspired Systems*, Technion - Israel Institute of Technology, Haifa, Israel, March 2012.

Memristors and Related Applications
- *The International Conference of the Israeli Semiconductor Industry (ChipEx 2011)*, Tel Aviv, Israel, May 2011.

<u>Posters</u>

1. **S. Kvatinsky**, E. G. Friedman, A. Kolodny and U.C. Weiser, "Memristor-based Applications," *1st Technion Computer Engineering (TCE) Conference*, June 2011.
2. **S. Kvatinsky**, E. G. Friedman, A. Kolodny and U.C. Weiser, "Memristor-based Circuits and Architectures," *2nd Technion Computer Engineering (TCE) Conference*, June 2012.
3. **S. Kvatinsky**, E. G. Friedman, A. Kolodny and U.C. Weiser, "Memristor-based Logic," *MemCo Workshop - Memristors for Computing*, November 2012.
4. D. Soudry, D. Di Castro, A. Gal, A. Kolodny, and **S. Kvatinsky**, "Implementing Hebbian Learning Rules with Memristors," *Workshop on "Memristor-based Systems for Neuromorphic Applications,"* September 2013.

5. R. Ben-Hur and **S. Kvatinsky**, "Processing within a Memristive Memory," *Proceedings of the International Workshop on Emerging Memory Solutions, DATE Conference*, March 2016.
6. N. Wainstein and **S. Kvatinsky**, "RF Memristor Modeling," *International Conference on Memristive Materials, Devices & Systems*, April 2017.
7. E. Giacomin, T. Greenberg-Toledo, **S. Kvatinsky**, and P.-E. Gaillardon, "A Robust Digital RRAM-based Convolutional Block without Process Variation Dependencies," *Design Automation Conference*, June 2018.
8. L. Danial, Y. Roizin, and **S. Kvatinsky**, "Neuromorphic Data Converters Using Floating-Gate Memristive Devices," *Neuromorphic Computing – a Nature Conference*, October 2019. **Best poster award**
9. D. Bhattacharjee, A. Chattopadhyay, S. Dutta, R. Ronen, and **S. Kvatinsky**, "SCAR: A SCalable ARea-Constrained Technology Mapping Flow for MAGIC," *Design Automation Conference*, July 2020.
10. N. Wainstein, G. Akonina, **S. Kvatinsky**, and E. Yalon, "Electrothermal Compact Modeling of Indirectly Heated Phase Change RF Switches," *Device Research Conference*, June 2020.
11. K. Stern, N. Wainstein, Y. Keller, C. M. Neumann, E. Pop, **S. Kvatinsky**, and E. Yalon, "Sub-Nanosecond Partial Reset for Analog Phase Change Neuromorphic Devices," *Device Research Conference*, June 2021. ***Best student poster award***
12. O. Leitersdorf, R. Ronen, and **S. Kvatinsky**, "PartitionPIM: Practical Memristive Partitions for Fast Processing-in-Memory," *Design Automation Conference*, July 2022.
13. O. Leitersdorf, R. Ronen, and **S. Kvatinsky**, "Fast In-Memory Floating-Point Addition," *Design Automation Conference*, July 2022.
14. M. M. Dahan, E. T. Breyer, S. Slesazeck, T. Mikolajick, and **S. Kvatinsky**, "C-AND: Mixed Writing Scheme for Disturb Reduction in 1T Ferroelectric FET Memory," *The International Meeting on Ferroelectricity*, March 2023. ***Best poster award.***
15. T. Patni, R. Daniels, and **S. Kvatinsky**, "V-VTEAM: A Compact Behavioral Model for Volatile Memristors," *International Conference on Memristive Materials, Devices and Systems*, November 2024.